

ZZZ1

PCB
DAZ@

PJP1

45@DCIN

ZZZ2

LA-5981P
DA2@

ZZZ3

LS-5981P
DA2@

ZZZ4

LS-5982P
DA2@

ZZZ5

LS-5983P
DA2@

ZZZ6

LS-5984P
DA2@

ZZZ7

LS-5986P
DA2@

Compal Confidential

NCQF0 M/B Schematics Document

Intel Arrandale/Clarkfield Processor with DDRIII + Ibex Peak-M

2010-04-18

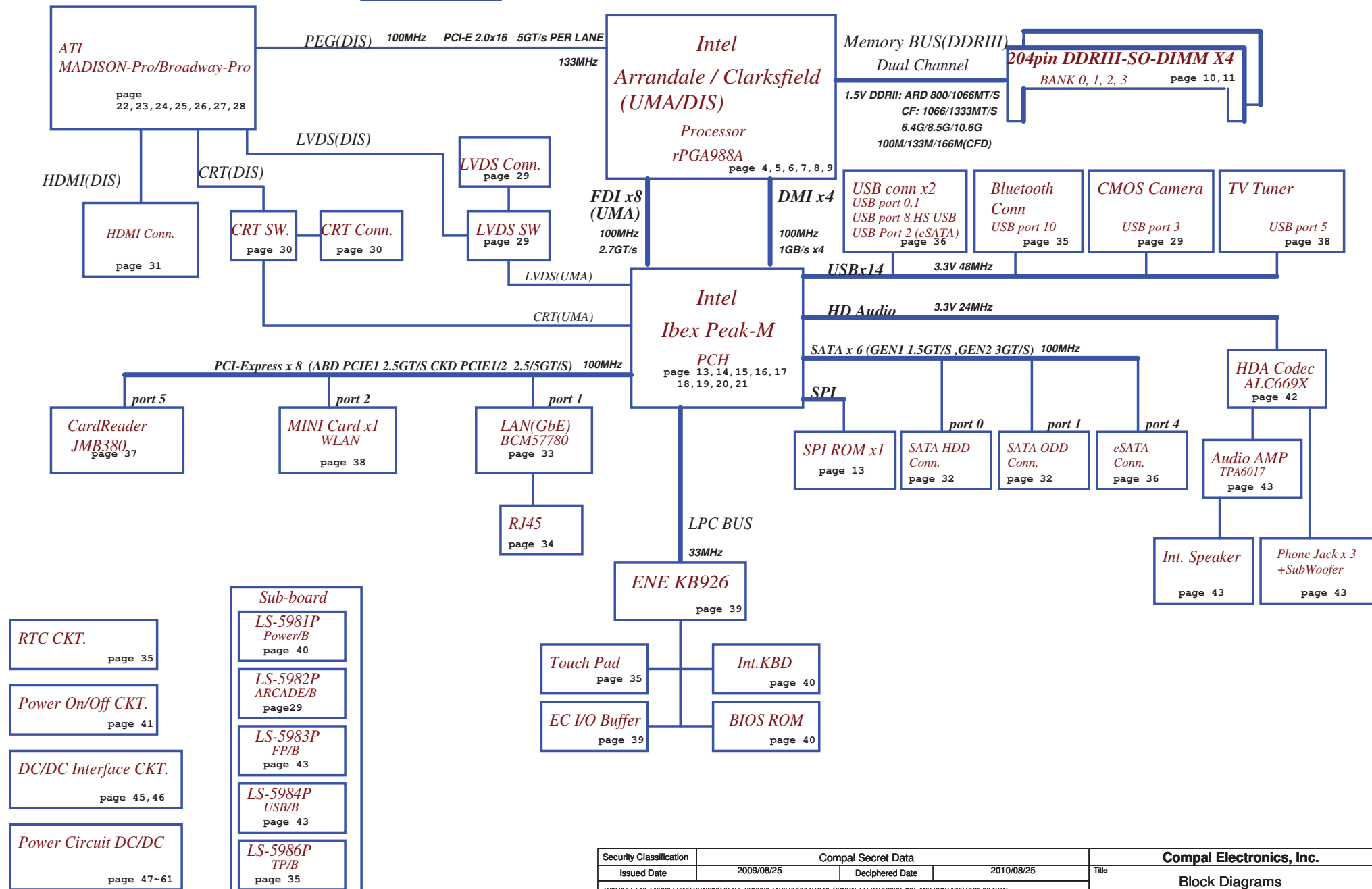
REV : 1 . A

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				Date	Sunday, April 18, 2010
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Model Name : NCQF0
File Name : LA5981P

Fan Control page 44

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
27MHz no SSC to VGA



Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSb always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG85P587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727	0101 1100b
ISL90728	0111 1100b

Board ID / SKU ID Table for AD channel

BOARD ID Table

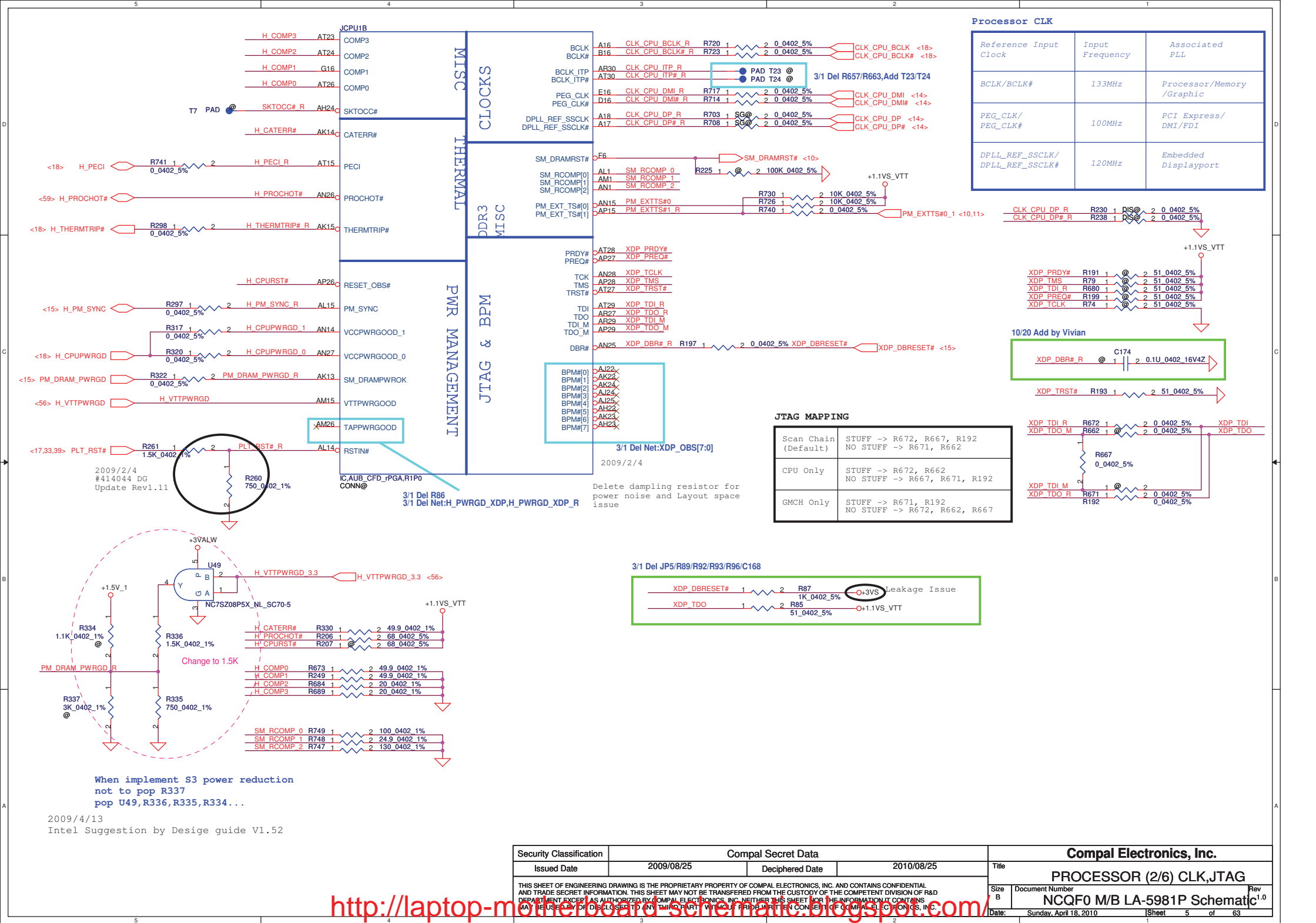
BTO Option Table

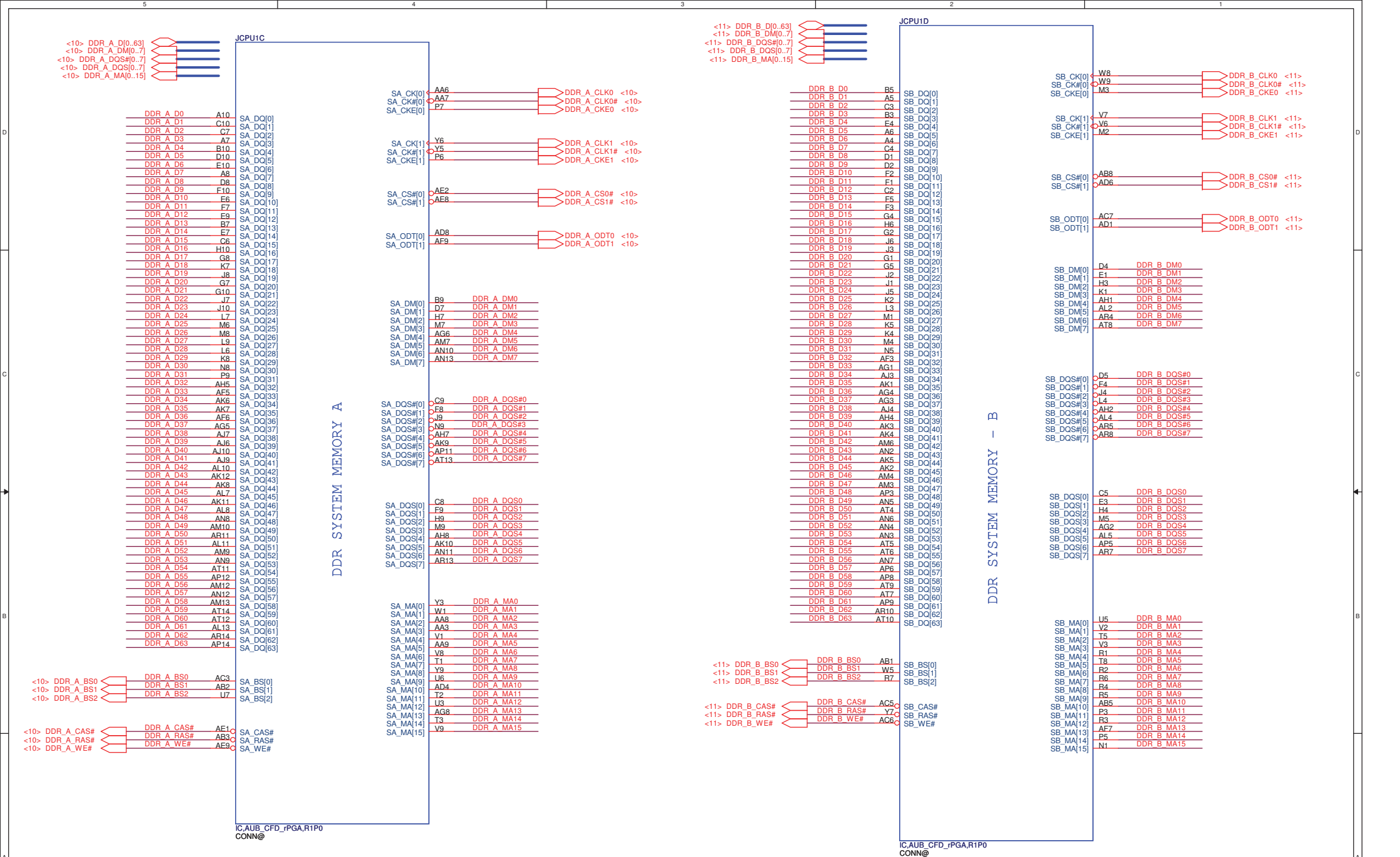
BOM Config

USB Port Table

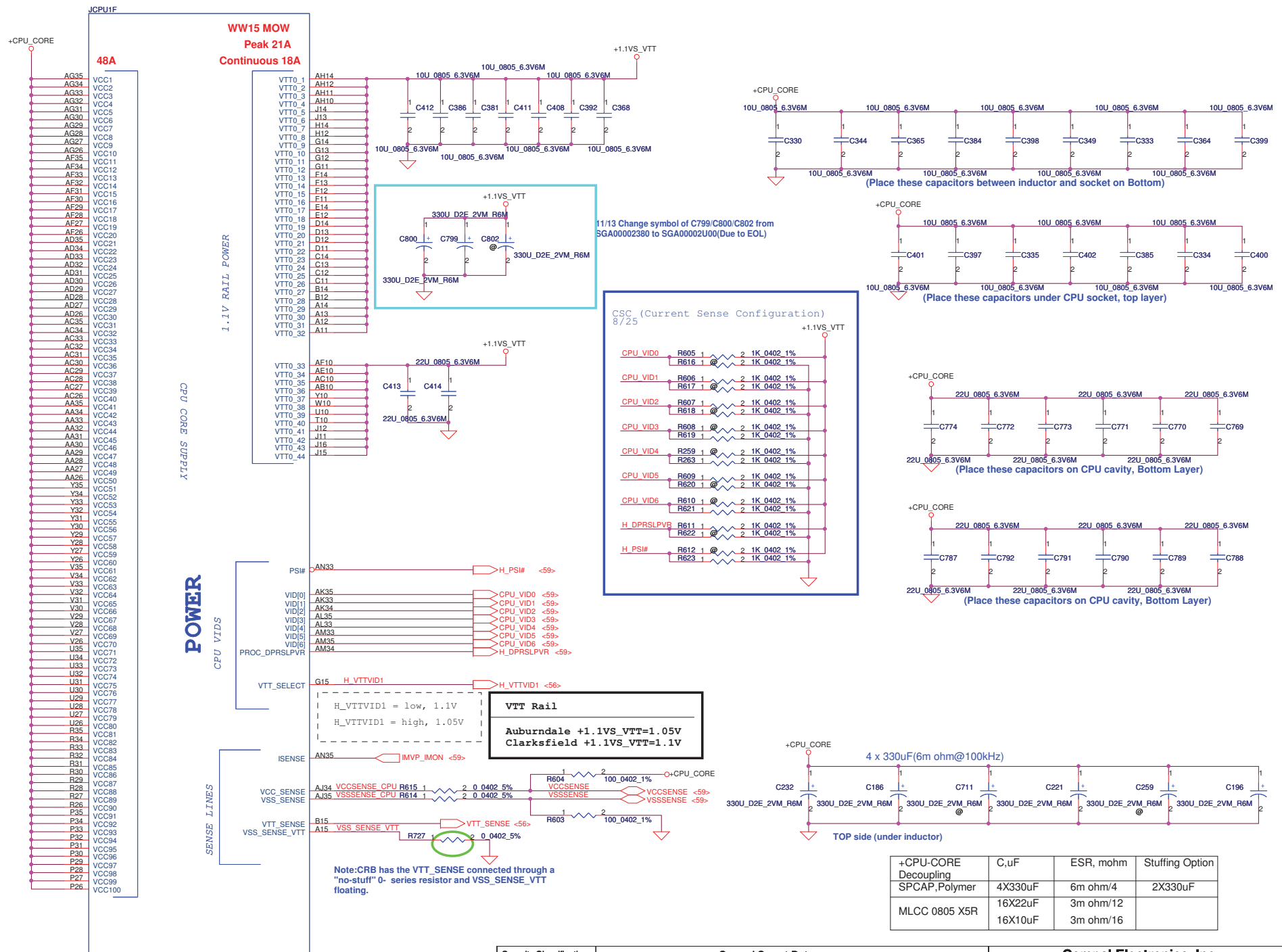
USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

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				Notes List			
Size B		Document Number		Rev		NCQF0 M/B LA-5981P Schematic ⁰	
Date:		Sunday, April 18, 2010		Sheet		3 of 63	



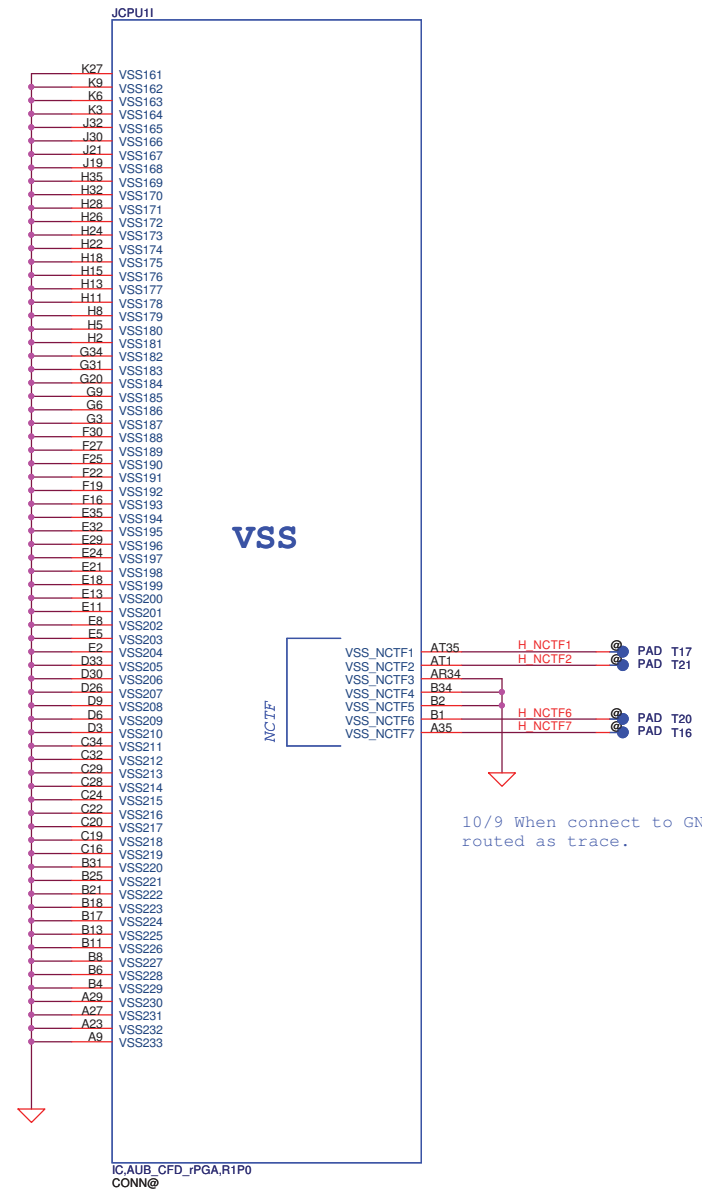
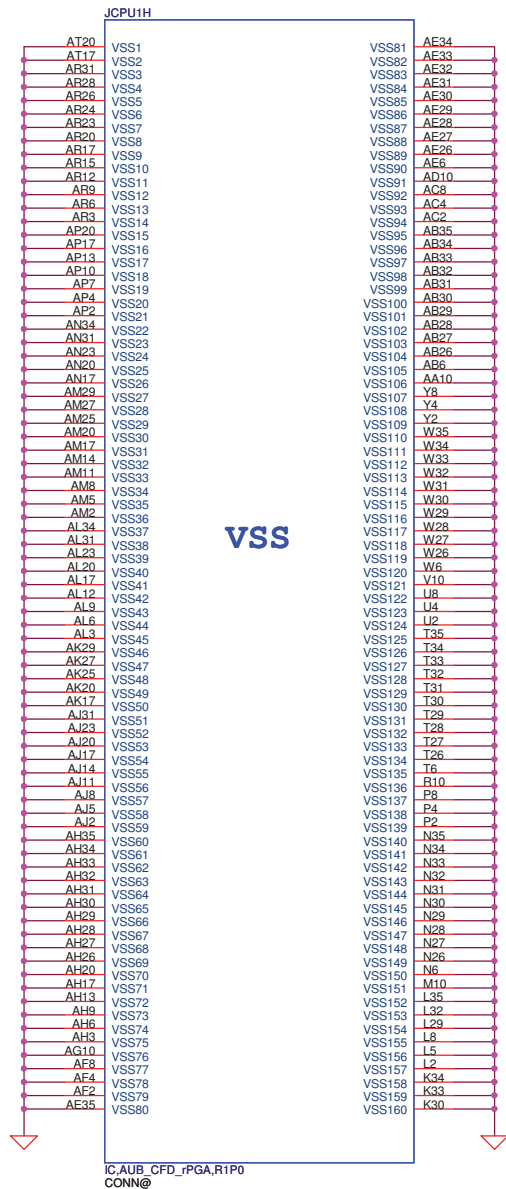


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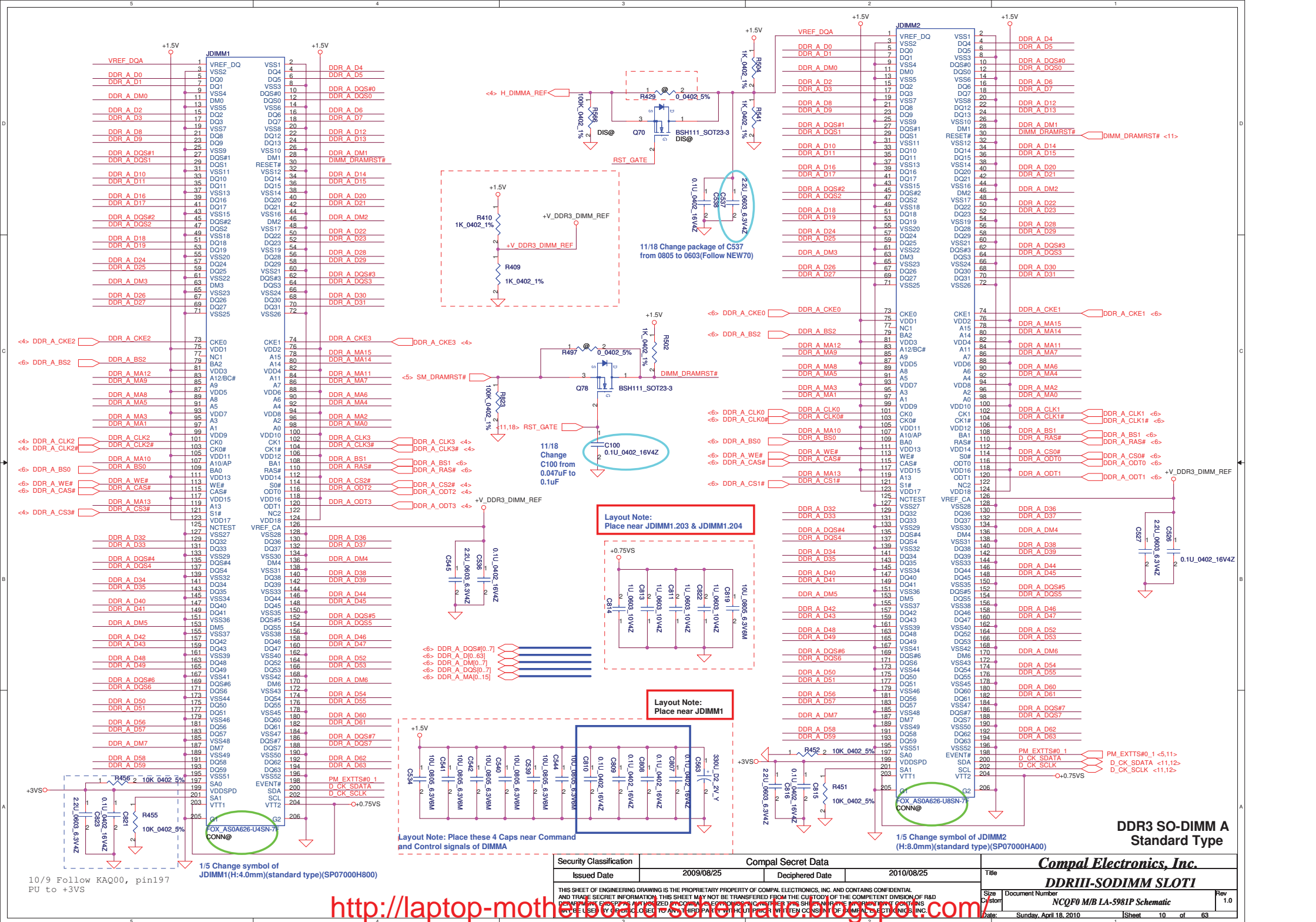
IC_AUB_CFD_PGA_R1P0
CONN@

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						Size	Document Number	Rev
						Custom	NCQF0 M/B LA-5981P Schematic	
Date:		Sunday, April 18, 2010		Sheet		9 of 63		

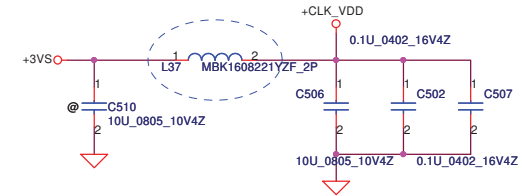
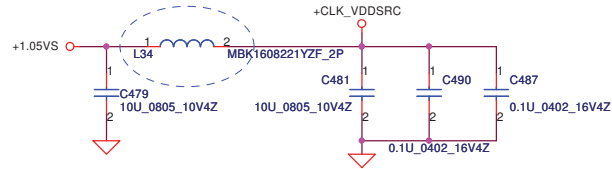
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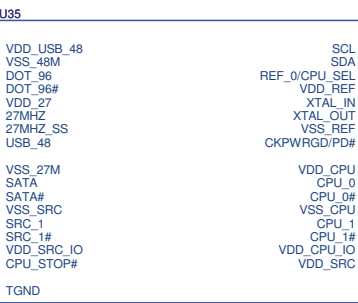
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10/9 Change L39 part number
from SM010014520 to SM01000AX00

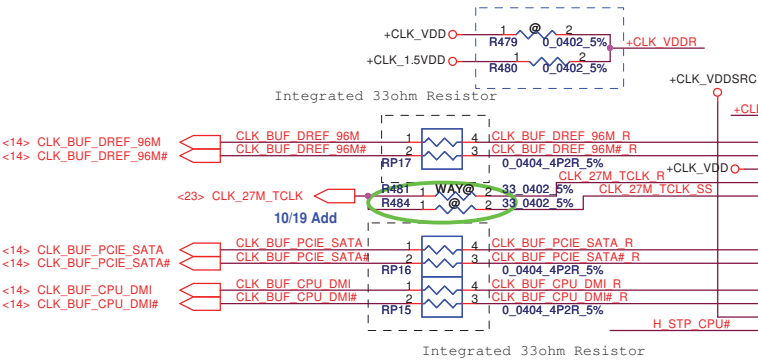


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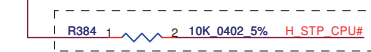
Clock Generator



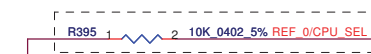
9LVS3199AKLFT_32P
12/11 Change PN of U35 to SA00003HR00
LOW Power:
Realtek: RTM890N-631-VB-GRT, SA00003HQ10
*IDT: ICS9LVS3199AKLFT, SA00003HR00



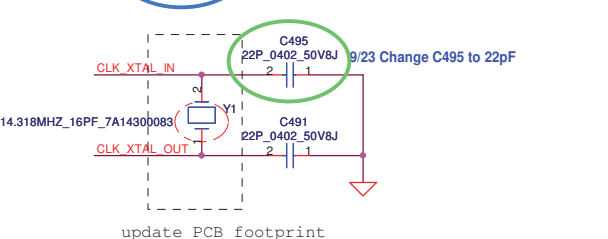
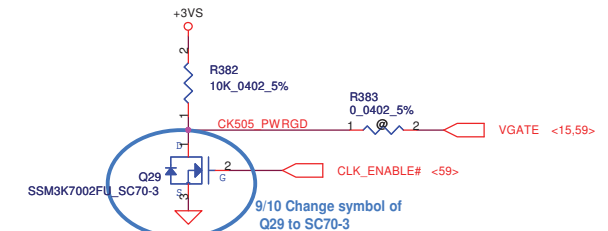
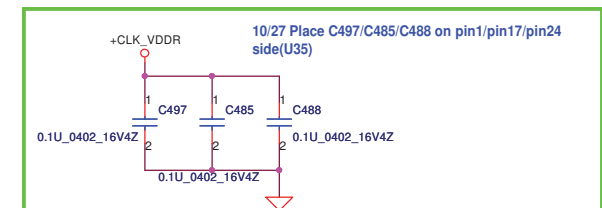
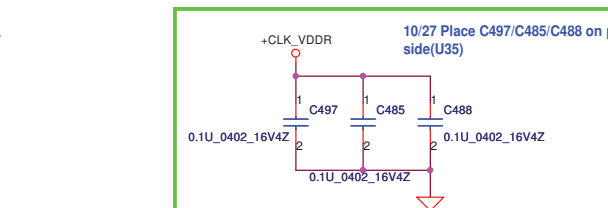
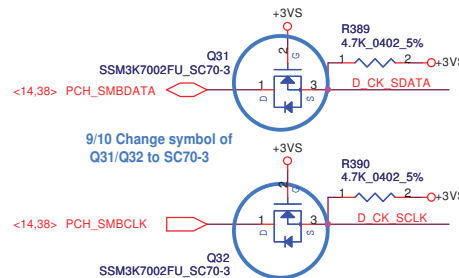
Silego Have Internal Pull-Up



IDT Have Internal Pull-Down



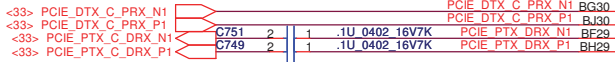
PIN	30	CPU_0	CPU_1
0 (Default)		133MHz	133MHz
1		100MHz	100MHz



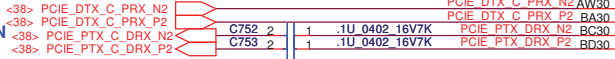
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				Size		
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Customer				NCQF0 M/B LA-5981P Schematic		
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For PCIE LAN



For Wireless LAN

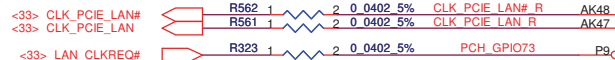


For CardReader

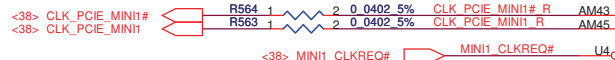


2/10 PCIE7, PCIE8 not support on HM55

For PCIE LAN



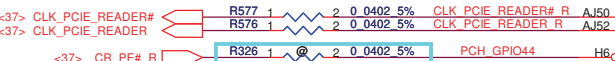
For Wireless LAN



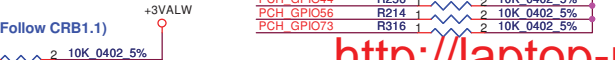
For Mini2



For CardReader



9/14 Change to +3VALW(Follow CRB1.1)



9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

REV1.0

PCI-E*

From CLK BUFFER

Clock Flex

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PCH (2/9) PCIE, SMBUS, CLK

Size

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2010/08/25

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Size

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9/14 Change PN of U60 from SA00002KV0L to SA00003NI20

U60C

REV1.0

DMI_HTX_PRX_N0 BC24
DMI_HTX_PRX_N1 BJ22
DMI_HTX_PRX_N2 AW20
DMI_HTX_PRX_N3 BJ20

DMI_HTX_PRX_P0 BD24
DMI_HTX_PRX_P1 BG22
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DMI_HTX_PRX_P3 BG20

DMI_PTX_HRX_N0 BE22
DMI_PTX_HRX_N1 BF21
DMI_PTX_HRX_N2 BD20
DMI_PTX_HRX_N3 BE18

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DMI_PTX_HRX_P1 BH21
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DMI2RXN
DMI3RXN

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DMI2RXP
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FDI_RXN6
FDI_RXN7

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FDI_RXP2
FDI_RXP3
FDI_RXP4
FDI_RXP5
FDI_RXP6
FDI_RXP7

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FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

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FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1

BA18 H_FDI_TXN0
BH17 H_FDI_TXN1
BD16 H_FDI_TXN2
BJ16 H_FDI_TXN3
BA16 H_FDI_TXN4
BE14 H_FDI_TXN5
BA14 H_FDI_TXN6
BG12 H_FDI_TXN7

BB18 H_FDI_TXP0
BE17 H_FDI_TXP1
BC16 H_FDI_TXP2
BG16 H_FDI_TXP3
AW16 H_FDI_TXP4
BD14 H_FDI_TXP5
BB14 H_FDI_TXP6
BD12 H_FDI_TXP7

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H_FDI_TXN5
H_FDI_TXN6
H_FDI_TXN7

H_FDI_TXP0
H_FDI_TXP1
H_FDI_TXP2
H_FDI_TXP3
H_FDI_TXP4
H_FDI_TXP5
H_FDI_TXP6
H_FDI_TXP7

H_FDI_TXN0
H_FDI_TXN1
H_FDI_TXN2
H_FDI_TXN3
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H_FDI_TXN7

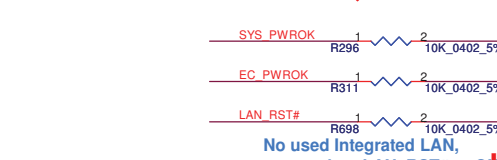
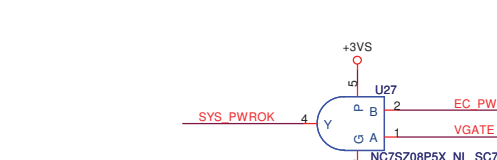
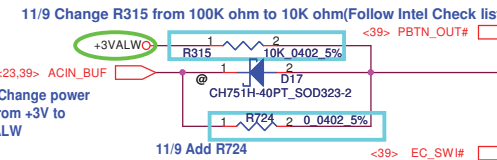
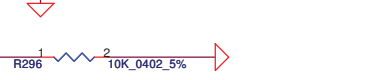
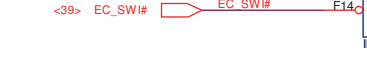
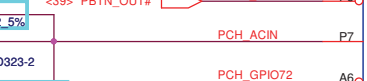
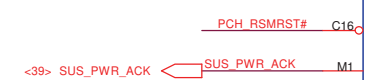
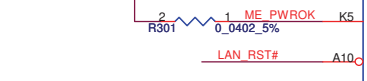
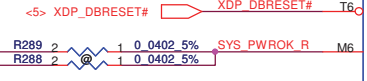
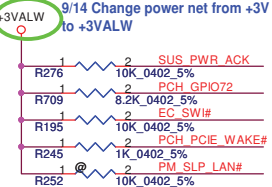
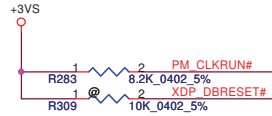
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H_FDI_TXN2
H_FDI_TXN3
H_FDI_TXN4
H_FDI_TXN5
H_FDI_TXN6
H_FDI_TXN7

H_FDI_TXP0
H_FDI_TXP1
H_FDI_TXP2
H_FDI_TXP3
H_FDI_TXP4
H_FDI_TXP5
H_FDI_TXP6
H_FDI_TXP7

H_FDI_TXN0
H_FDI_TXN1
H_FDI_TXN2
H_FDI_TXN3
H_FDI_TXN4
H_FDI_TXN5
H_FDI_TXN6
H_FDI_TXN7

H_FDI_TXP0
H_FDI_TXP1
H_FDI_TXP2
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H_FDI_TXP6
H_FDI_TXP7

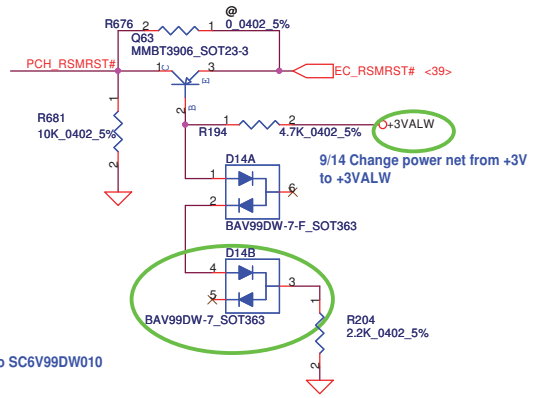
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H_FDI_TXN2
H_FDI_TXN3
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H_FDI_TXN5
H_FDI_TXN6
H_FDI_TXN7



System Power Management

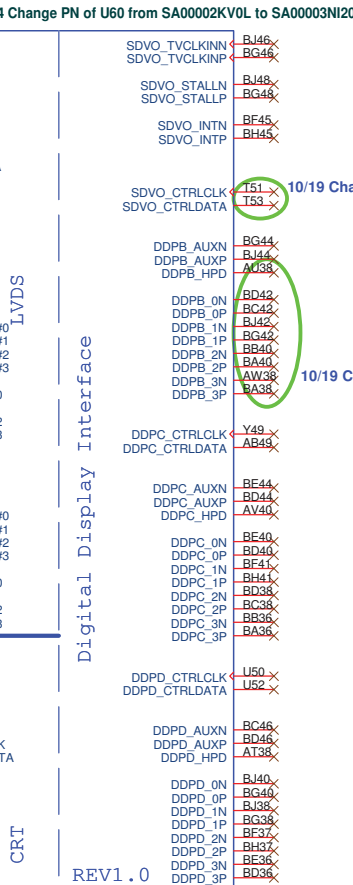
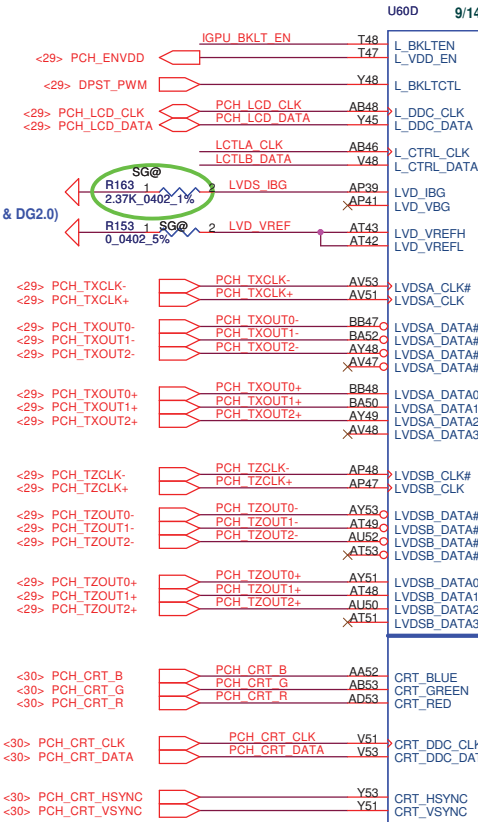
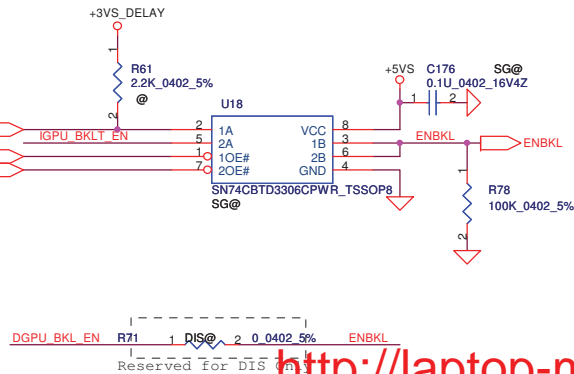
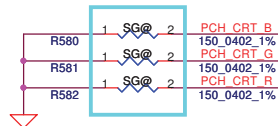
IBEXPEAK-M_FCBGA107

9/14 Change PN of D14B from SC6V99DW000 to SC6V99DW010



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/08/25				Deciphered Date			
2010/08/25				2010/08/25				Title			
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Document Number				NCQF0 M/B LA-5981P Schematic				Rev			
Date				Sunday, April 18, 2010				Sheet			
15				63				of			

12/11 Change Bom structure of R580/R581/R582/R111/R112/RR89/R590 from mount to SG@

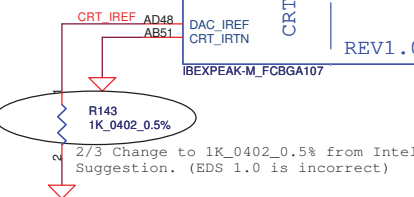


Digital Display Interface

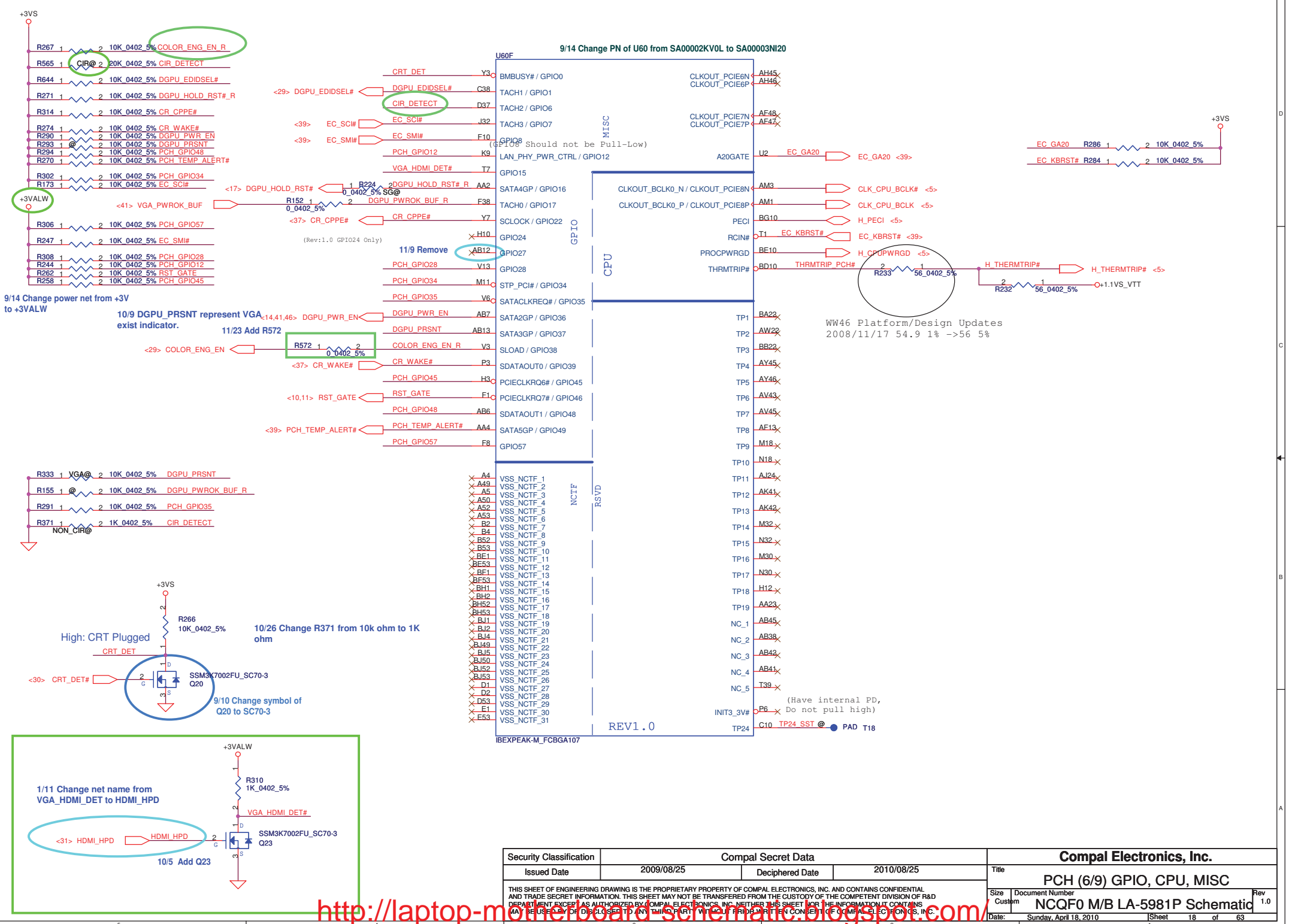
REV1.0

10/19 Change to NC(by Vivian)

10/19 Change to NC(by Vivian)



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	PCH (4/9) LVDS, CRT, DPI
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				Document Number	NCQF0 M/B LA-5981P Schematic
				Date	Sunday, April 18, 2010
				Sheet	16 of 63
				Rev	1.0



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Issued Date		2009/08/25		Deciphered Date		2010/08/25		Title		
								PCH (6/9) GPIO, CPU, MISC		
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								Custom	NCQF0 M/B LA-5981P Schematic	1.0
Date:		Sunday, April 18, 2010		Sheet		18		of 63		



AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BQ12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	M38
BB42	VSS[178]	VSS[278]	M38
BB49	VSS[179]	VSS[279]	M42
BB5	VSS[180]	VSS[280]	M46
BC10	VSS[181]	VSS[281]	M49
BC14	VSS[182]	VSS[282]	M5
BC18	VSS[183]	VSS[283]	M8
BC2	VSS[184]	VSS[284]	N24
BC22	VSS[185]	VSS[285]	P11
BC32	VSS[186]	VSS[286]	AD23
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	AD32
BD9	VSS[191]	VSS[291]	AD34
BD48	VSS[192]	VSS[292]	AD22
BD5	VSS[193]	VSS[293]	P42
BE12	VSS[194]	VSS[294]	P47
BE16	VSS[195]	VSS[295]	R2
BE24	VSS[196]	VSS[296]	R52
BE30	VSS[197]	VSS[297]	T12
BE34	VSS[198]	VSS[298]	AE4
BE38	VSS[199]	VSS[299]	AE4
BE42	VSS[200]	VSS[300]	AE4
BE46	VSS[201]	VSS[301]	AE4
BE48	VSS[202]	VSS[302]	AE4
BE50	VSS[203]	VSS[303]	AE4
BE52	VSS[204]	VSS[304]	AE4
BE54	VSS[205]	VSS[305]	AE4
BE56	VSS[206]	VSS[306]	AE4
BE58	VSS[207]	VSS[307]	AE4
BE6	VSS[208]	VSS[308]	AE4
BE64	VSS[209]	VSS[309]	AE4
BE68	VSS[210]	VSS[310]	AE4
BE72	VSS[211]	VSS[311]	AE4
BE74	VSS[212]	VSS[312]	AE4
BE78	VSS[213]	VSS[313]	AE4
BE80	VSS[214]	VSS[314]	AE4
BE82	VSS[215]	VSS[315]	AE4
BE84	VSS[216]	VSS[316]	AE4
BE86	VSS[217]	VSS[317]	AE4
BE88	VSS[218]	VSS[318]	AE4
BE90	VSS[219]	VSS[319]	AE4
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BE94	VSS[221]	VSS[321]	AE4
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BE100	VSS[224]	VSS[324]	AE4
BE102	VSS[225]	VSS[325]	AE4
BE104	VSS[226]	VSS[326]	AE4
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BE108	VSS[228]	VSS[328]	AE4
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BE112	VSS[230]	VSS[330]	AE4
BE114	VSS[231]	VSS[331]	AE4
BE116	VSS[232]	VSS[332]	AE4
BE118	VSS[233]	VSS[333]	AE4
BE120	VSS[234]	VSS[334]	AE4
BE122	VSS[235]	VSS[335]	AE4
BE124	VSS[236]	VSS[336]	AE4
BE126	VSS[237]	VSS[337]	AE4
BE128	VSS[238]	VSS[338]	AE4
BE130	VSS[239]	VSS[339]	AE4
BE132	VSS[240]	VSS[340]	AE4
BE134	VSS[241]	VSS[341]	AE4
BE136	VSS[242]	VSS[342]	AE4
BE138	VSS[243]	VSS[343]	AE4
BE140	VSS[244]	VSS[344]	AE4
BE142	VSS[245]	VSS[345]	AE4
BE144	VSS[246]	VSS[346]	AE4
BE146	VSS[247]	VSS[347]	AE4
BE148	VSS[248]	VSS[348]	AE4
BE150	VSS[249]	VSS[349]	AE4
BE152	VSS[250]	VSS[350]	AE4
BE154	VSS[251]	VSS[351]	AE4
BE156	VSS[252]	VSS[352]	AE4
BE158	VSS[253]	VSS[353]	AE4
BE160	VSS[254]	VSS[354]	AE4
BE162	VSS[255]	VSS[355]	AE4
BE164	VSS[256]	VSS[356]	AE4
BE166	VSS[257]	VSS[357]	AE4
BE168	VSS[258]	VSS[358]	AE4

REV1.0
IBEXPEAK-M_FCBGA107
9/14 Change PN of U60 from SA00002KVOL to SA00003N20

AB16	VSS[0]	VSS[80]	AK30
AA19	VSS[1]	VSS[81]	AK31
AA20	VSS[2]	VSS[82]	AK32
AA22	VSS[3]	VSS[83]	AK33
AA24	VSS[4]	VSS[84]	AK34
AA26	VSS[5]	VSS[85]	AK35
AA28	VSS[6]	VSS[86]	AK36
AA30	VSS[7]	VSS[87]	AK37
AA32	VSS[8]	VSS[88]	AK38
AA34	VSS[9]	VSS[89]	AK39
AA36	VSS[10]	VSS[90]	AK40
AA38	VSS[11]	VSS[91]	AK41
AA40	VSS[12]	VSS[92]	AK42
AA42	VSS[13]	VSS[93]	AK43
AA44	VSS[14]	VSS[94]	AK44
AA46	VSS[15]	VSS[95]	AK45
AA48	VSS[16]	VSS[96]	AK46
AA50	VSS[17]	VSS[97]	AK47
AA52	VSS[18]	VSS[98]	AK48
AA54	VSS[19]	VSS[99]	AK49
AA56	VSS[20]	VSS[100]	AK50
AA58	VSS[21]	VSS[101]	AK51
AA60	VSS[22]	VSS[102]	AK52
AA62	VSS[23]	VSS[103]	AK53
AA64	VSS[24]	VSS[104]	AK54
AA66	VSS[25]	VSS[105]	AK55
AA68	VSS[26]	VSS[106]	AK56
AA70	VSS[27]	VSS[107]	AK57
AA72	VSS[28]	VSS[108]	AK58
AA74	VSS[29]	VSS[109]	AK59
AA76	VSS[30]	VSS[110]	AK60
AA78	VSS[31]	VSS[111]	AK61
AA80	VSS[32]	VSS[112]	AK62
AA82	VSS[33]	VSS[113]	AK63
AA84	VSS[34]	VSS[114]	AK64
AA86	VSS[35]	VSS[115]	AK65
AA88	VSS[36]	VSS[116]	AK66
AA90	VSS[37]	VSS[117]	AK67
AA92	VSS[38]	VSS[118]	AK68
AA94	VSS[39]	VSS[119]	AK69
AA96	VSS[40]	VSS[120]	AK70
AA98	VSS[41]	VSS[121]	AK71
AA100	VSS[42]	VSS[122]	AK72
AA102	VSS[43]	VSS[123]	AK73
AA104	VSS[44]	VSS[124]	AK74
AA106	VSS[45]	VSS[125]	AK75
AA108	VSS[46]	VSS[126]	AK76
AA110	VSS[47]	VSS[127]	AK77
AA112	VSS[48]	VSS[128]	AK78
AA114	VSS[49]	VSS[129]	AK79
AA116	VSS[50]	VSS[130]	AK80
AA118	VSS[51]	VSS[131]	AK81
AA120	VSS[52]	VSS[132]	AK82
AA122	VSS[53]	VSS[133]	AK83
AA124	VSS[54]	VSS[134]	AK84
AA126	VSS[55]	VSS[135]	AK85
AA128	VSS[56]	VSS[136]	AK86
AA130	VSS[57]	VSS[137]	AK87
AA132	VSS[58]	VSS[138]	AK88
AA134	VSS[59]	VSS[139]	AK89
AA136	VSS[60]	VSS[140]	AK90
AA138	VSS[61]	VSS[141]	AK91
AA140	VSS[62]	VSS[142]	AK92
AA142	VSS[63]	VSS[143]	AK93
AA144	VSS[64]	VSS[144]	AK94
AA146	VSS[65]	VSS[145]	AK95
AA148	VSS[66]	VSS[146]	AK96
AA150	VSS[67]	VSS[147]	AK97
AA152	VSS[68]	VSS[148]	AK98
AA154	VSS[69]	VSS[149]	AK99
AA156	VSS[70]	VSS[150]	AK100
AA158	VSS[71]	VSS[151]	AK101
AA160	VSS[72]	VSS[152]	AK102
AA162	VSS[73]	VSS[153]	AK103
AA164	VSS[74]	VSS[154]	AK104
AA166	VSS[75]	VSS[155]	AK105
AA168	VSS[76]	VSS[156]	AK106
AA170	VSS[77]	VSS[157]	AK107
AA172	VSS[78]	VSS[158]	AK108
AA174	VSS[79]	VSS[159]	AK109

REV1.0
IBEXPEAK-M_FCBGA107
9/14 Change PN of U60 from SA00002KVOL to SA00003N20

1. dGPU Power On at Post

- (1) Check DGPU_PRSENT (GPIO37) is low
- (2) Hold DGPU_HOLD_RST# (GPIO16) low, and wait for 100ms
- (3) Set DGPU_PWR_EN (GPIO36) high, and wait for 100ms
- (4) If, after 100 ms, VGA_PWROK_BUF (GPIO17) is not asserted high, then it is a fatal error
- (5) Set DGPU_HOLD_RST# pin high and wait 100ms
- (6) DGPU_SELECT is high

2. dGPU Power On at Runtime

- (1) 3 interposer
I. DGPU_HOLD_RST# held low
II. DGPU_PWR_EN held high to turn on dGPU
III. Delay 300ms
- (2) DGPU_HOLD_RST# held high

3. dGPU Power OFF at Runtime

- (1) Set DGPU_HOLD_RST# low
- (2) Set DGPU_PWR_EN low

DGPU_PWR_EN:
-Driven by BIOS to turn on/off discrete graphic power.

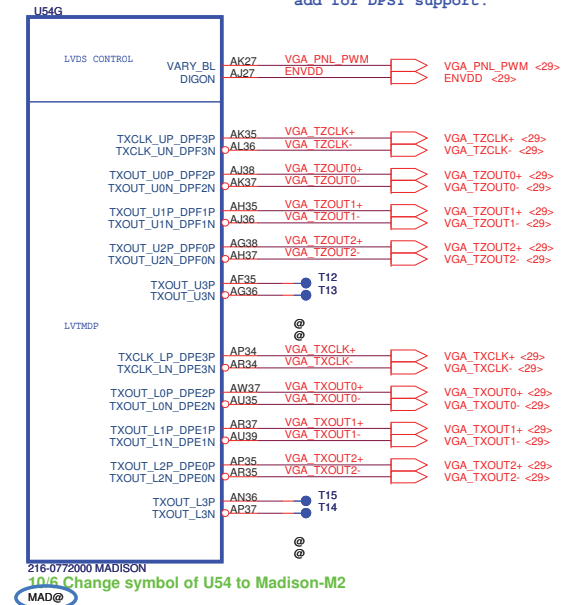
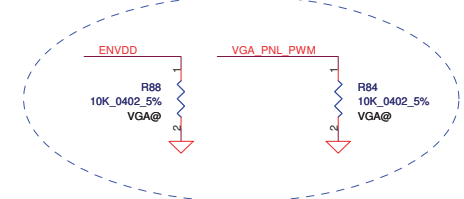
VGA_PWROK_BUF:
-Driven by dGPU VR to indicate the power status to PCH.
-Used to enable clocks to dGPU.

DGPU_HOLD_RST#:
-Discrete Graphic Enable signal. Controlled by BIOS and driven by PCH GPIO.
-Used to gate with Platform Reset to enable the Reset for dGPU.

DGPU_SELECT:
-Select line for MUX to control the Display from iGPU or dGPU
-Needs to be controlled by BIOS.

DGPU_PWM_SELECT#
-Select line for MUX to control Backlight Inverter from iGPU or dGPU.

EDID_SELECT#
-Select line for MUX to control EDID from iGPU or dGPU.



9/14 Change poewr net to +1.0VSDGPU

<http://laptop-motherboard-schematics.blogspot.com/>

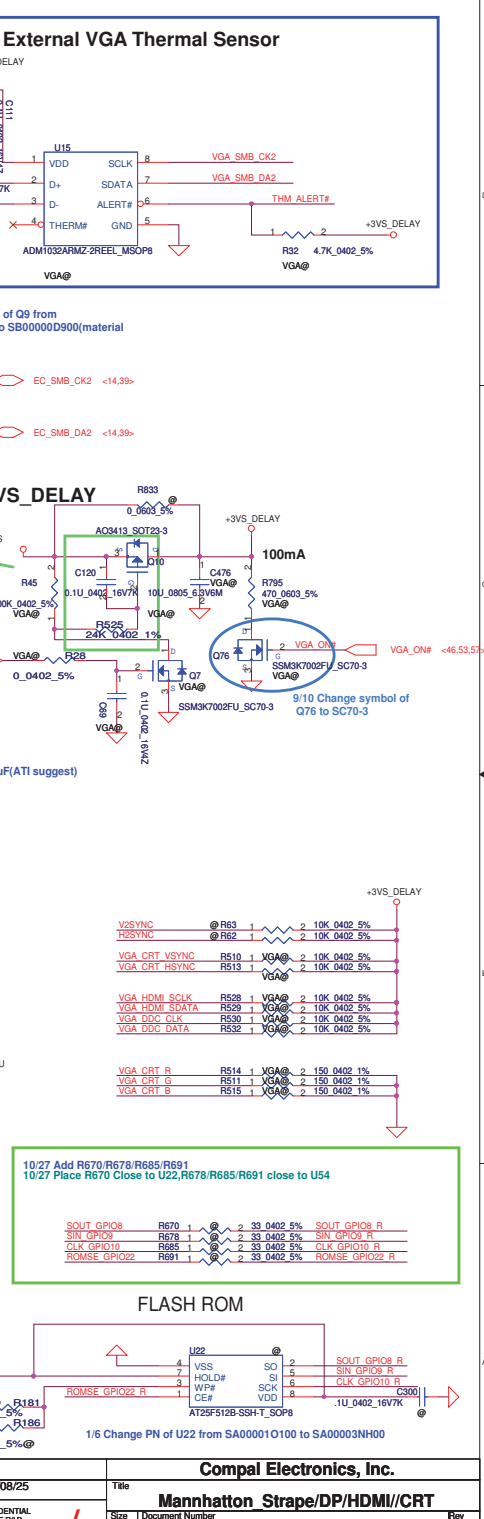
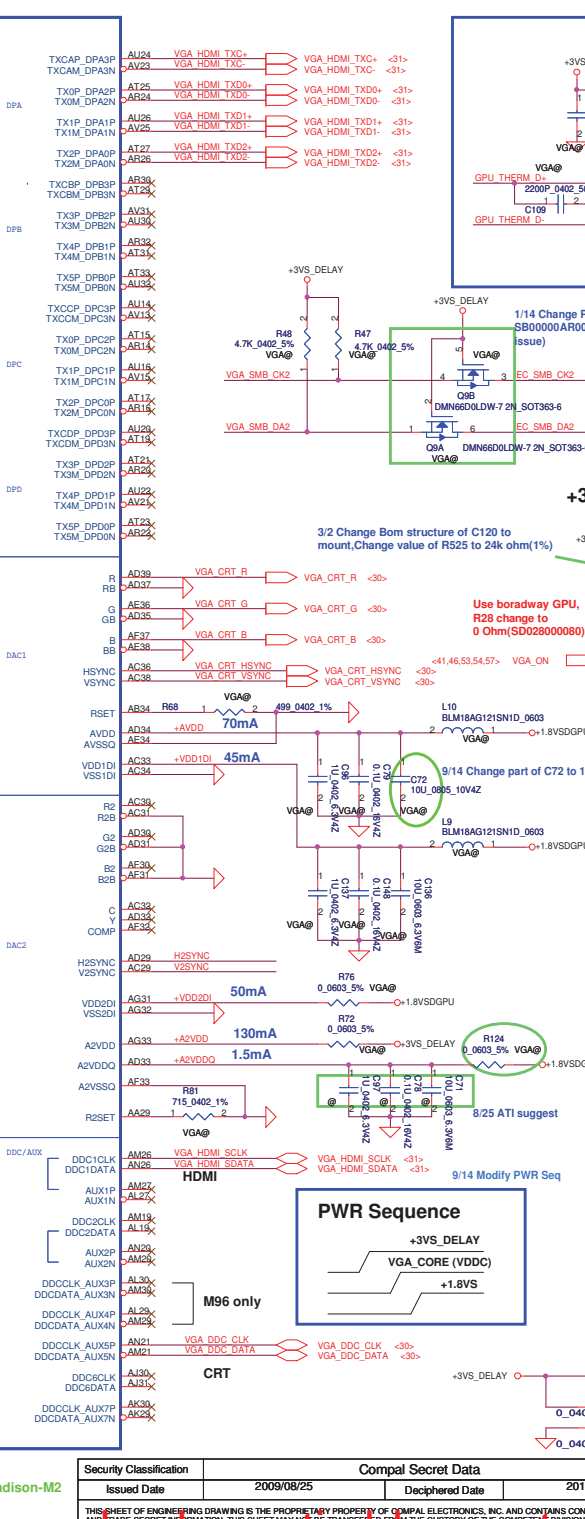
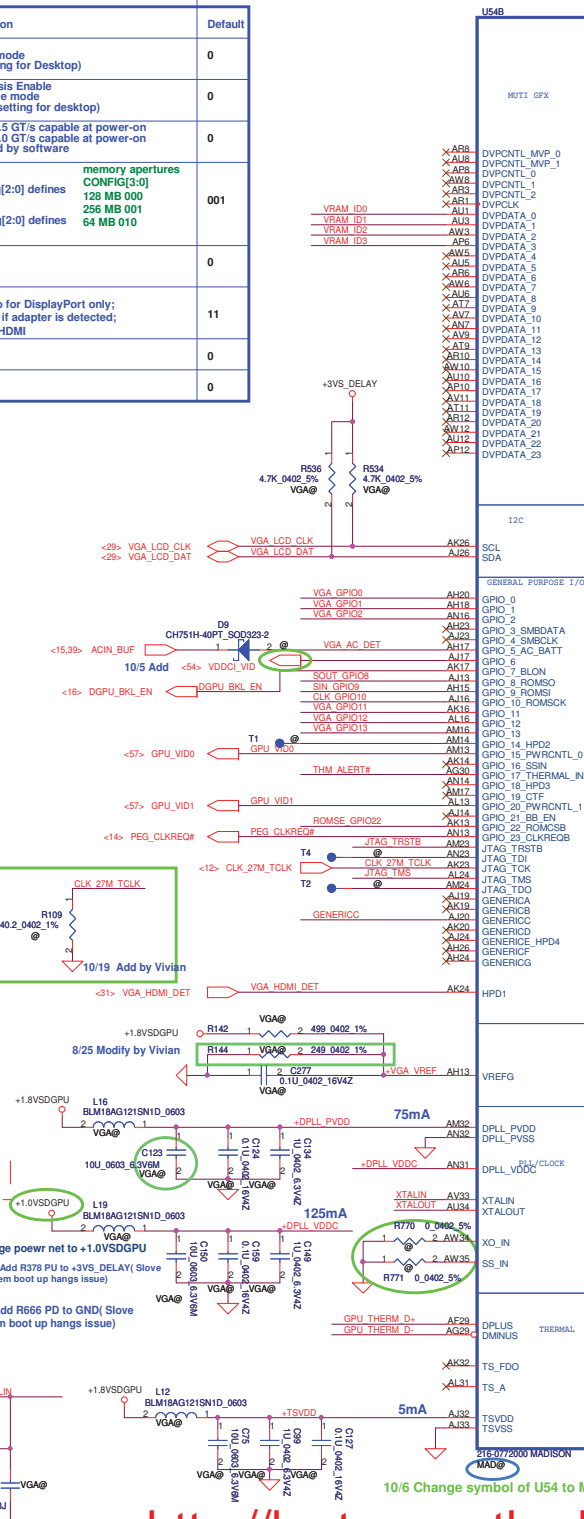
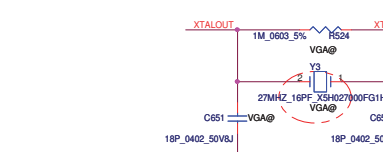
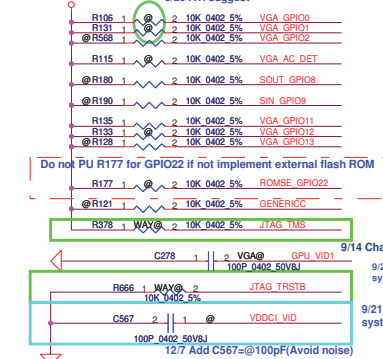
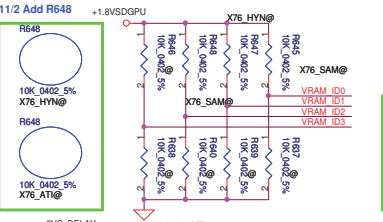
Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 01: Audio for DisplayPort only; 10: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

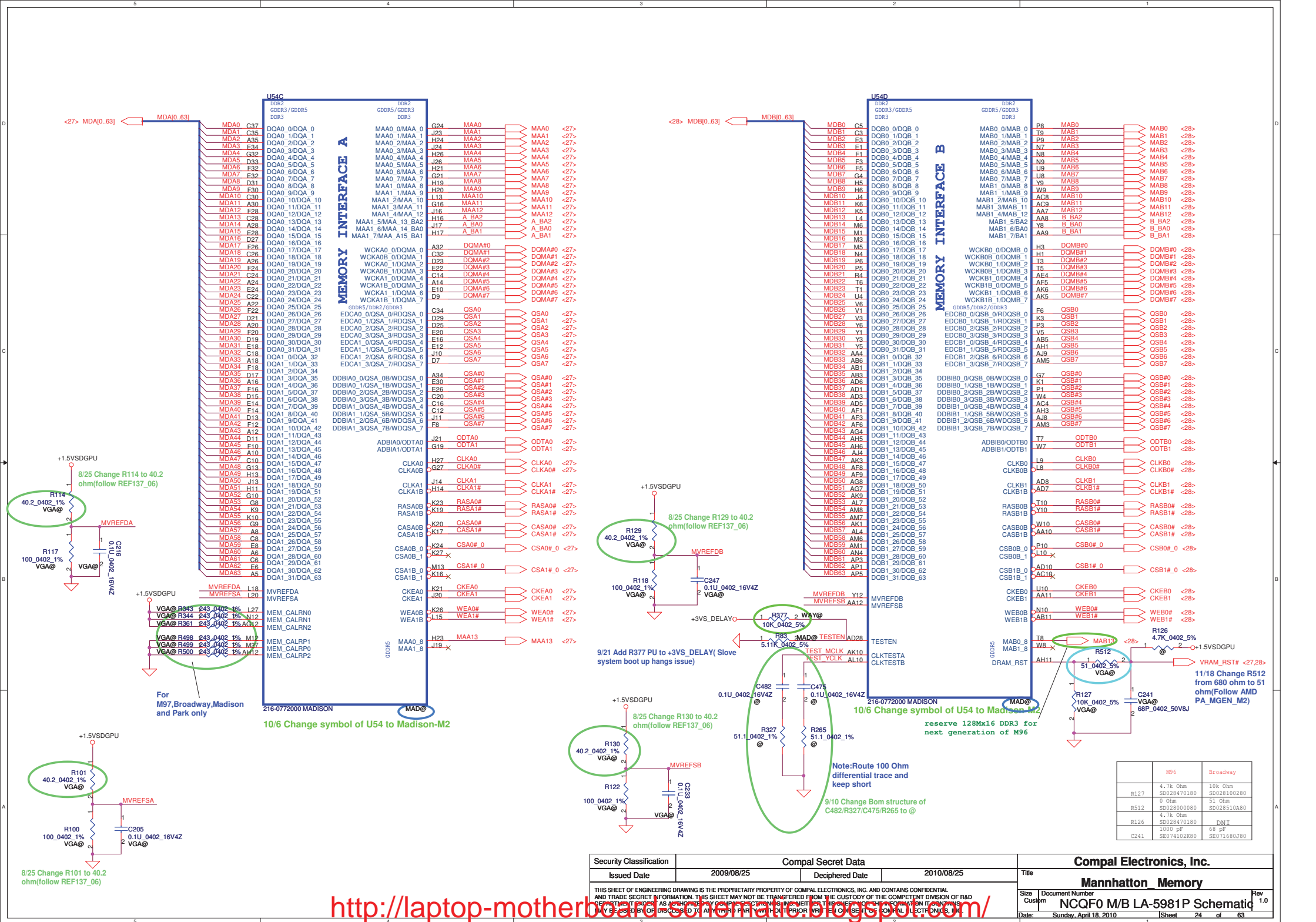
Madison Pro

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM				
ATI(8pcs)1GB	0	1	0	0
Samsung(8pcs)1GB	0	1	0	1
Hynix(8pcs)1GB	0	1	1	0
Samsung(8pcs)128*16	1	1	0	1
Hynix(8pcs)128*16	1	1	1	0

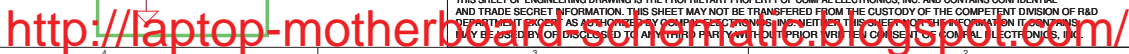
Broadway Pro

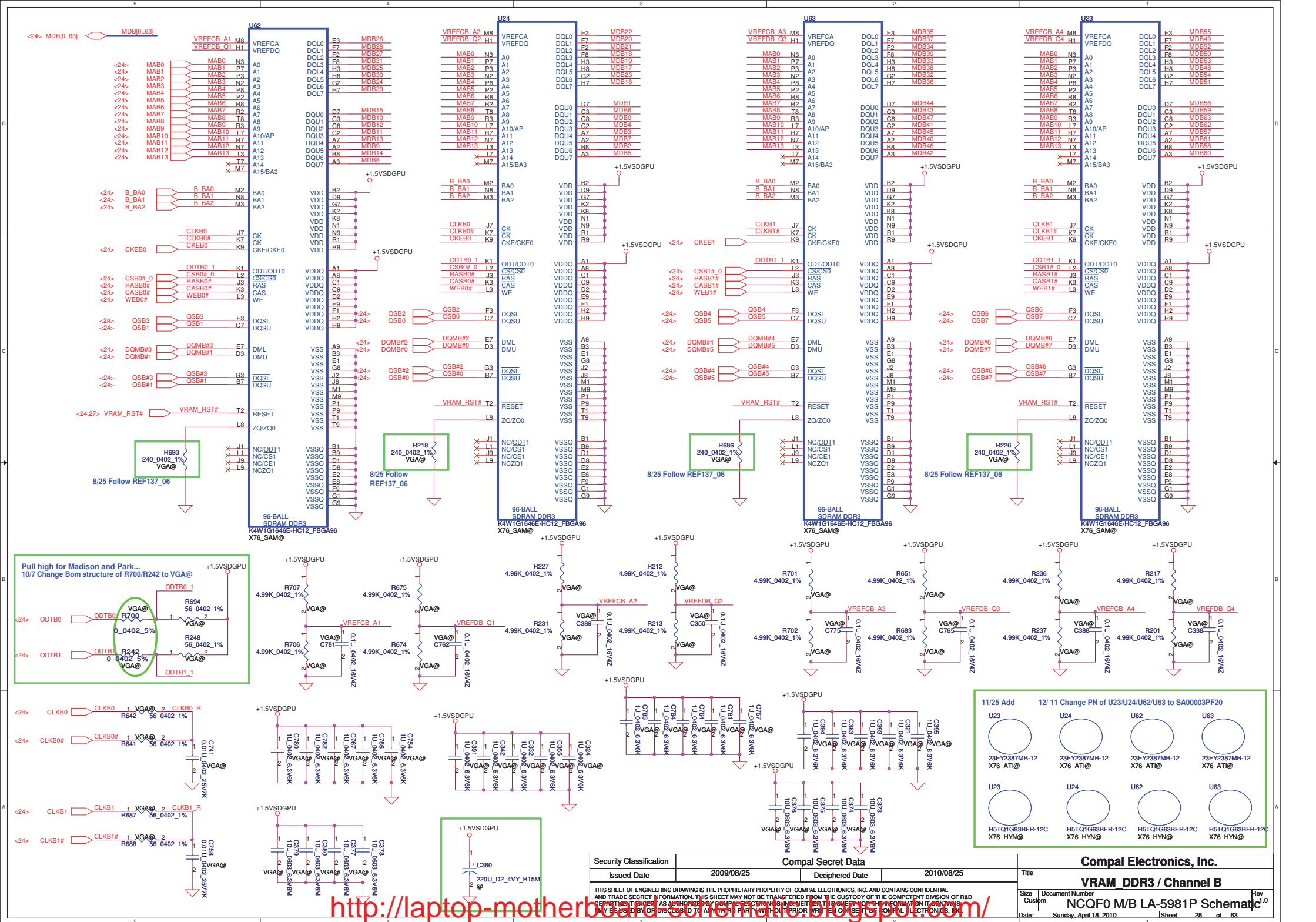
Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
VRAM				
ATI(8pcs)1GB	0	1	0	0
Samsung(8pcs)1GB	0	1	0	1
Hynix(8pcs)1GB	0	1	1	0
Samsung(8pcs)128*16	1	1	0	1
Hynix(8pcs)128*16	1	1	1	0



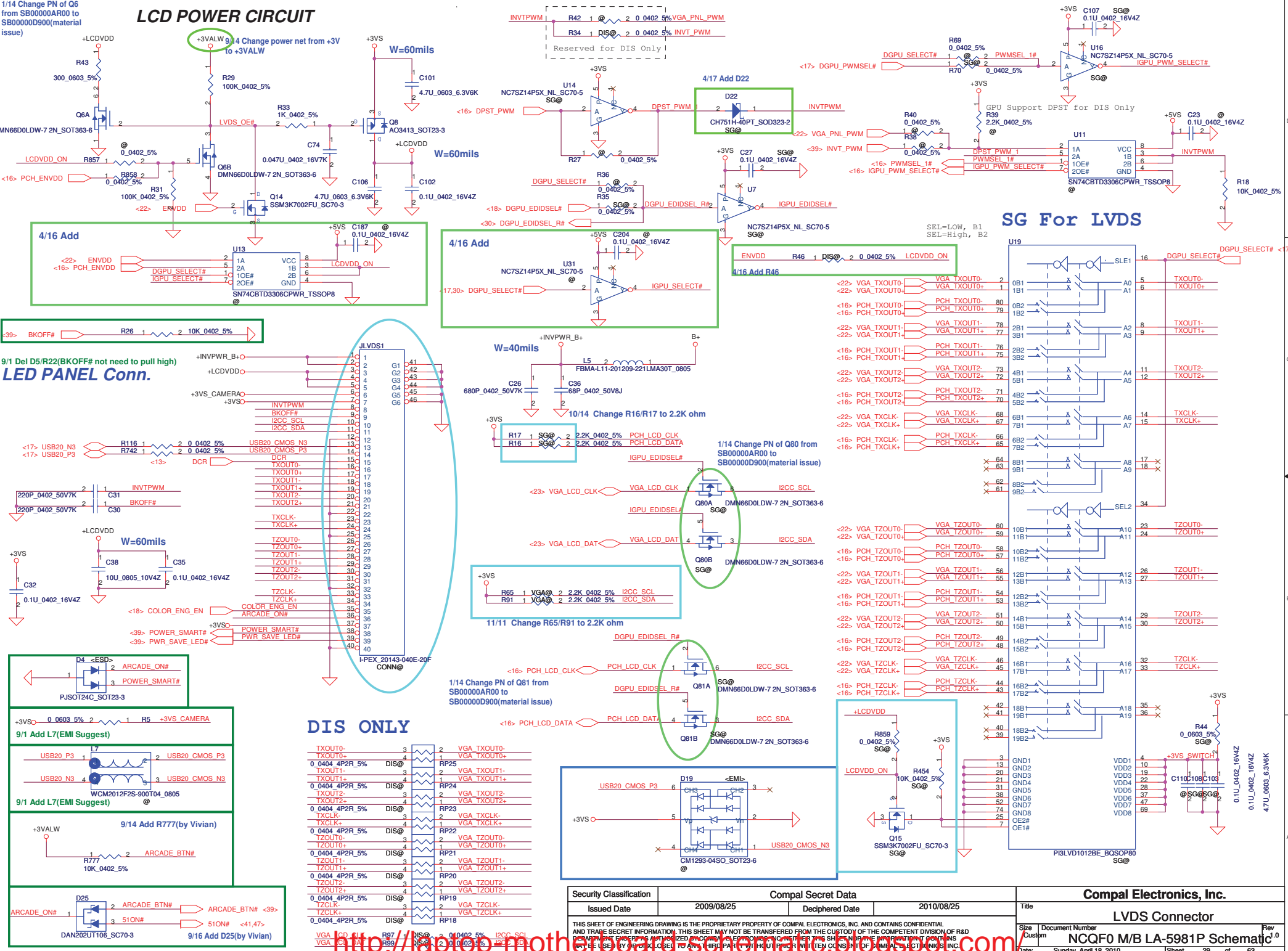








LCD POWER CIRCUIT

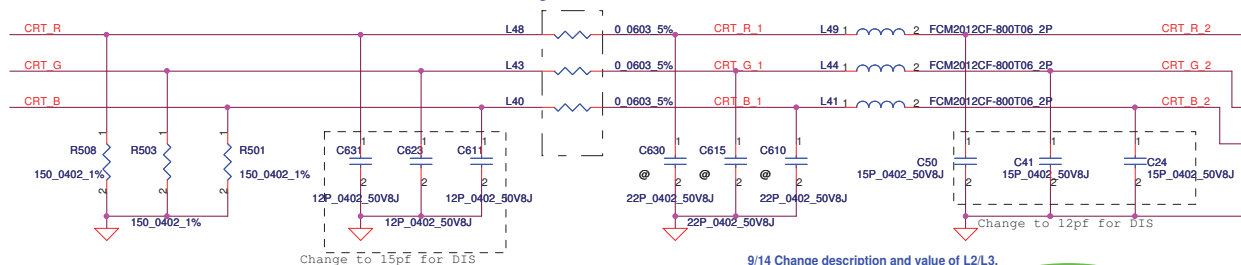


CRT Connector

10/14 Change PN of L40/L43/L48 to SM01000AX00

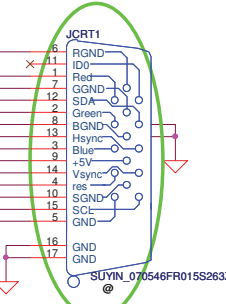
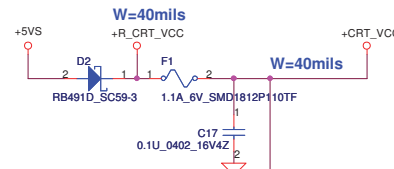
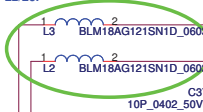


10/14 Change to 0 ohm for DIS

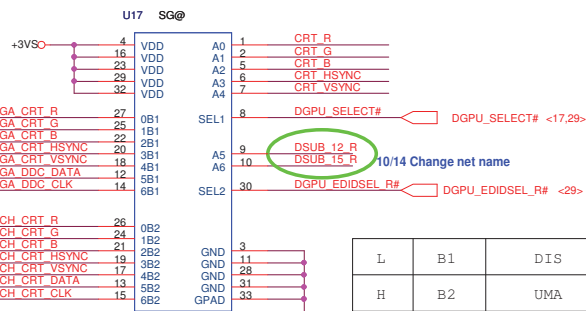
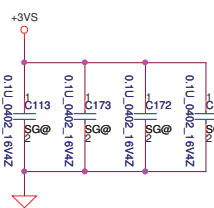


Change To 15pf for DIS

9/14 Change description and value of L2/L3.



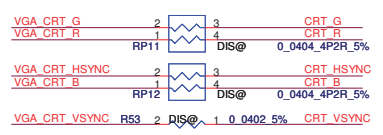
11/13 Change symbol of JCRT1 from DC060003O00 to DC060003N00



PI3V712-AZLEX_TOFN32_6X3-D

9/10 Change U17 from SA000026Y00 to SA00003B300
Michael

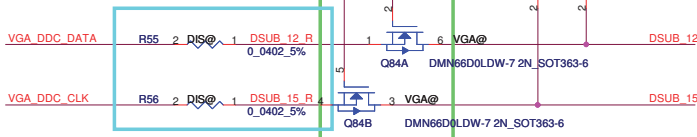
Reserved for DIS only



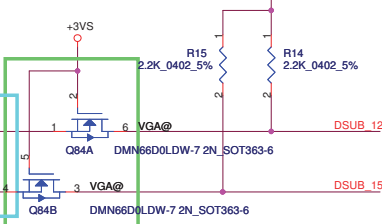
9/14 Change to RP for layout request
Michael

VGA DDC PU 4.7K
on Page 23
Reserved for DIS only

10/14 Add R55/R56= 0 ohm



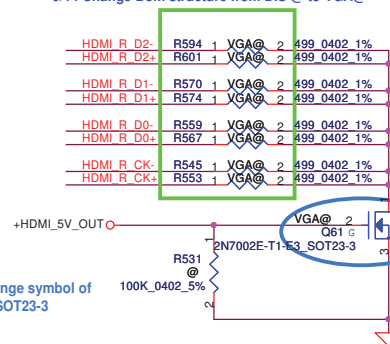
4/2 Change PN of Q84 from SB00000D900 to SB00000DH00(ESD issue)



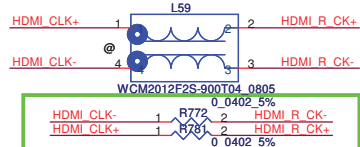
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Issued Date	2009/08/25	Deciphered Date	2009/08/25	CRT Connector	
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					NCQF0 M/B LA-5981P Schematic
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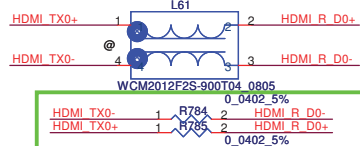
9/14 Change Bom structure from DIS @ to VGA@



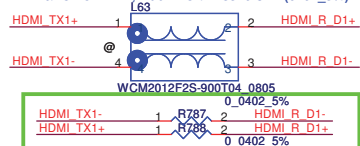
4/2 Change PN of Q61 from
SB570020110 to SB000008J10



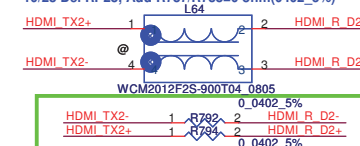
10/28 Del RP26, Add R772/R781=0 ohm(0402_5%)



10/28 Del RP27, Add R784/R785=0 ohm(0402_5

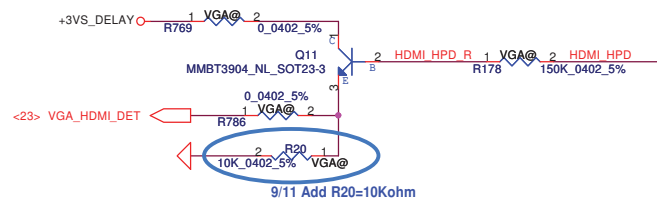


10/28 Del RP28, Add R787/R788=0 ohm(0402 5%)

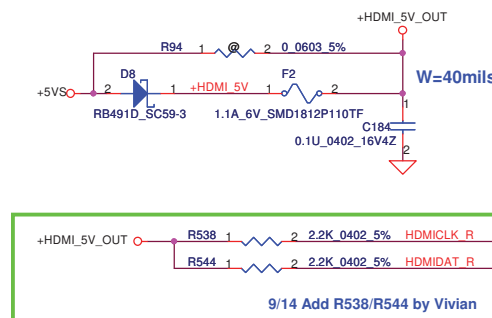


10/28 Del RP29, Add R792/R794=0 ohm(0402 5%)

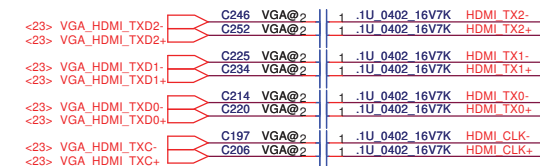
0914 Change to RP
Michael



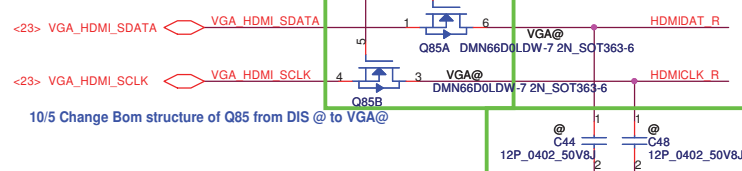
9/11 Add R20=10Kohm



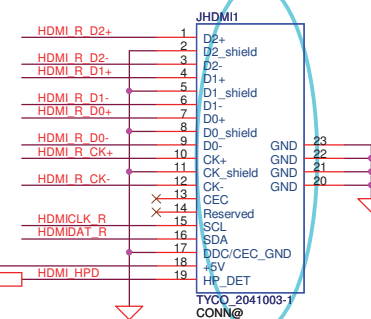
9/14 Add R538/R544 by Vivian



9/14 Change Bom structure of C44/C48 from DIS @ to @
1/14 Change PN of Q85 from
SB00000AR00 to SB00000D900(material
issue)



10/5 Change Bom structure of Q85 from DIS @ to VGA@

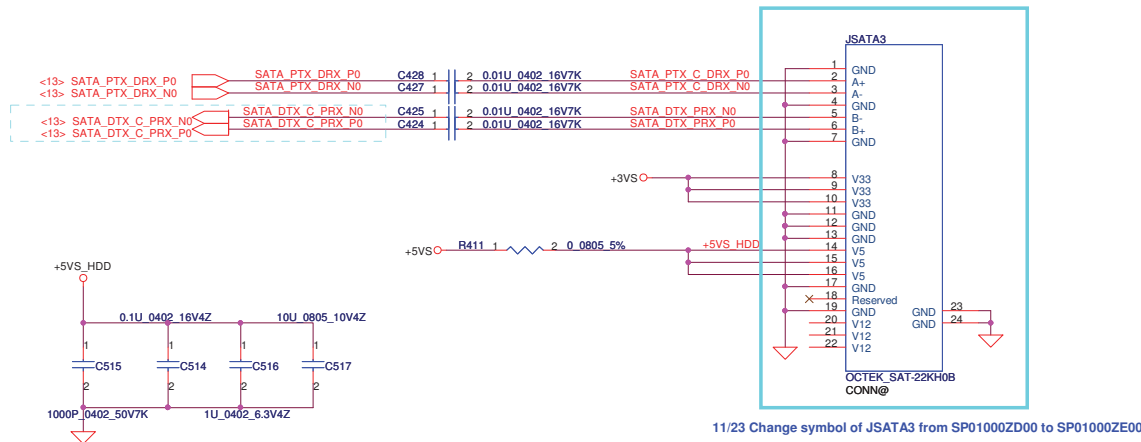


11/9 Change symbol of JHDMI1 from SP060003Z00 to DC232000A00

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				Size	Document Number	Rev
				Custom	NCQF0 M/B LA-5981P Schematic	1.0
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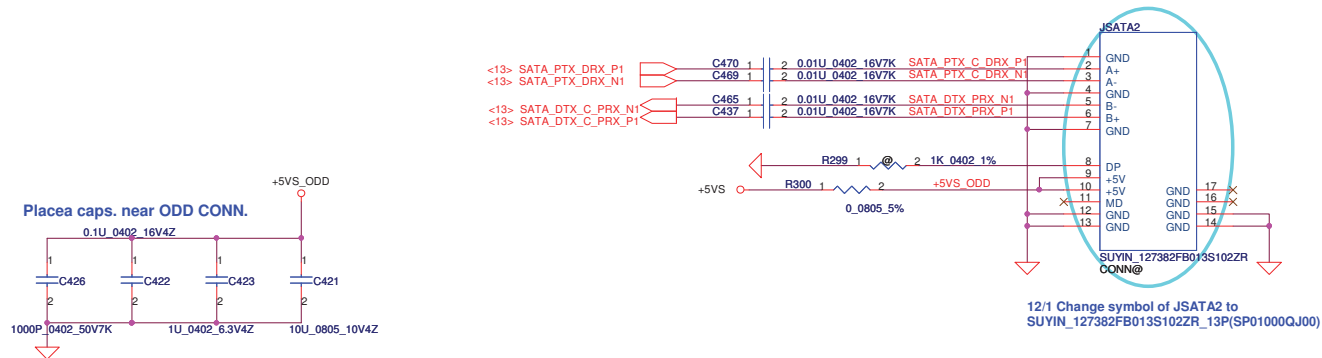
HDD

SATA HDD Conn.



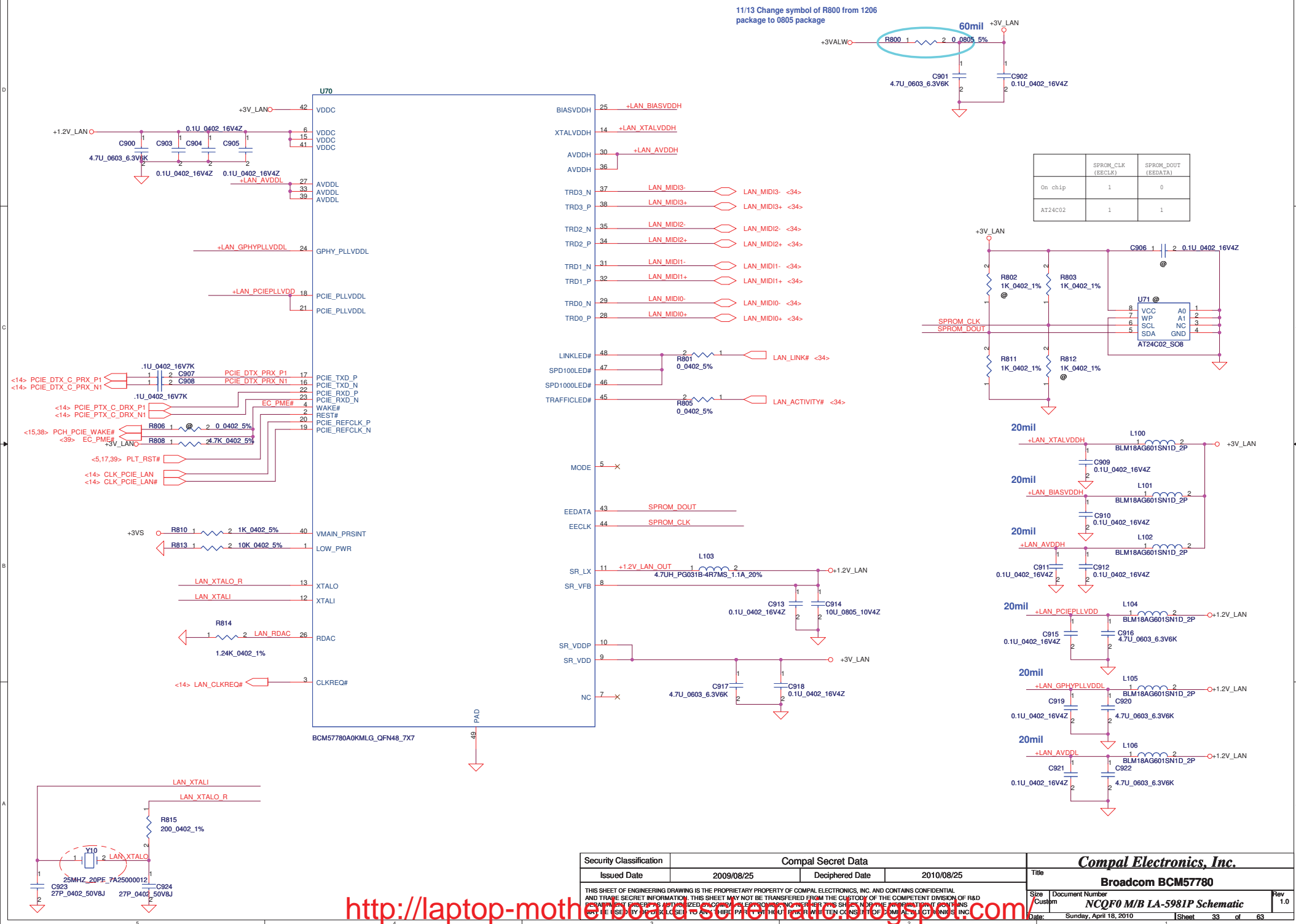
ODD

SATA ODD Conn.

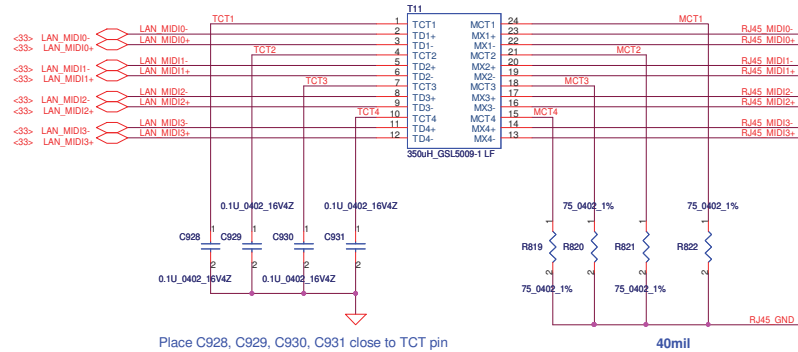


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				Date	NCQF0 M/B LA-5981P Schematic
				Sheet	32 of 63

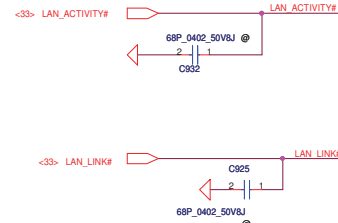
<http://laptop-motherboard-schematic.blogspot.com/>



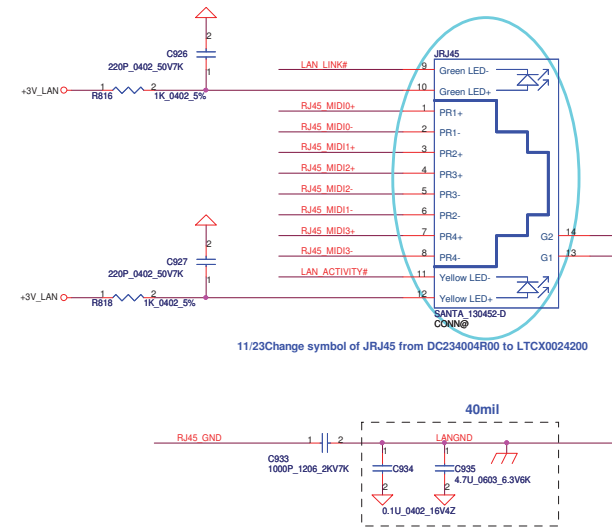
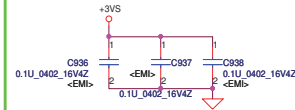
LAN Connector



0914 Swap LAN signals for layout routing
Michael



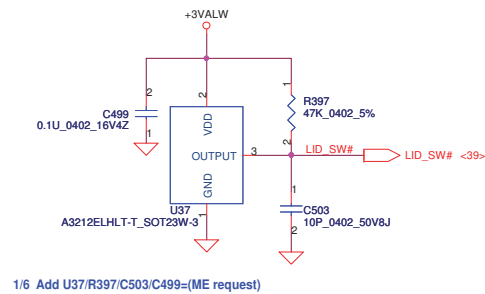
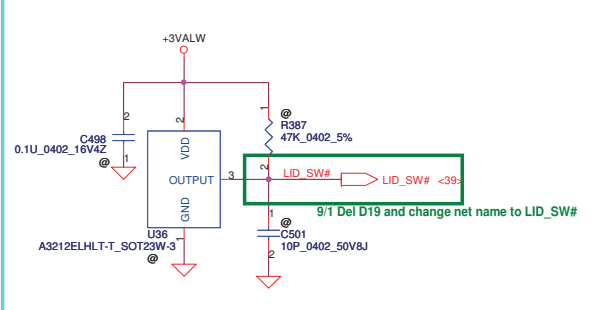
2/25 Add C936-C938(EMI request)



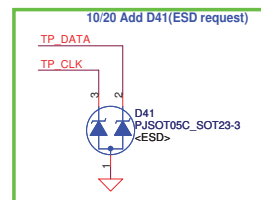
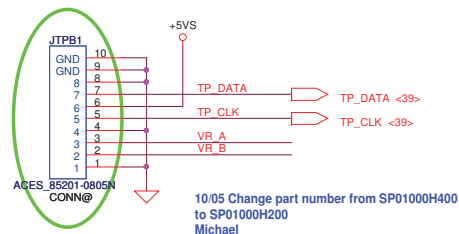
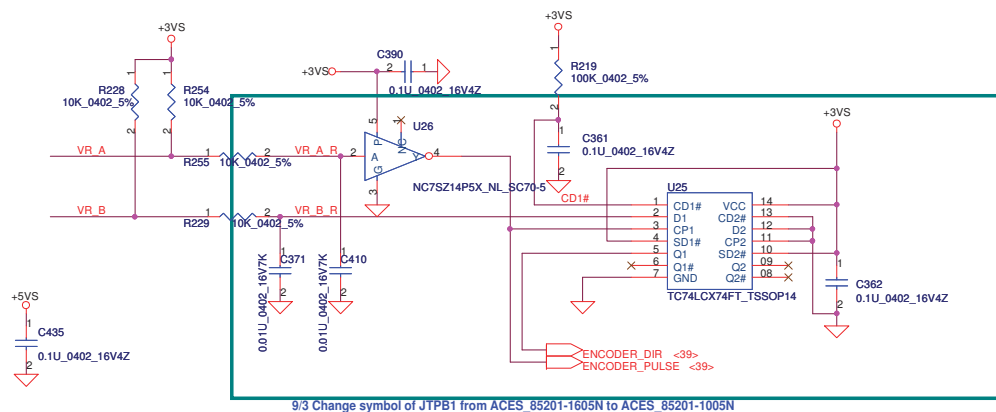
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2009/08/25	Deciphered Date	2010/08/25	LAN Magnetic & RJ45	
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Lid Switch

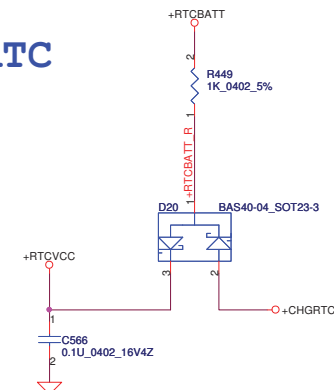
(Hall Effect Switch)



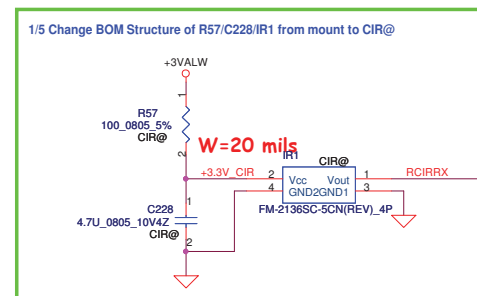
Touch Pad



RTC



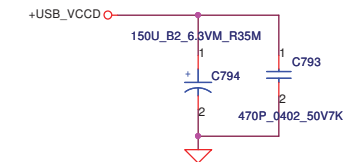
CIR



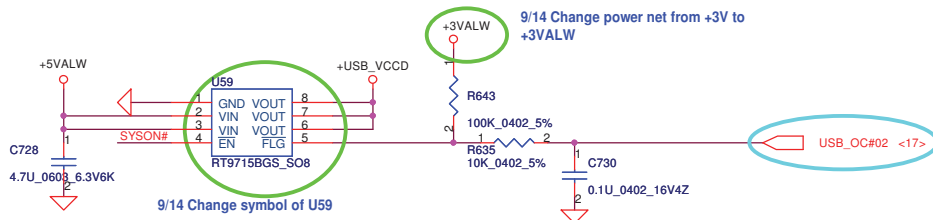
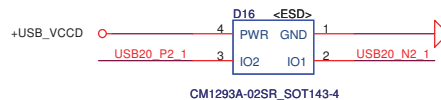
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				Deciphered Date				Title			
2009/08/25				2010/08/25				LID/RTC/CIR			
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Date				Document Number				1.0			
Sunday, April 18, 2010				NCQF0 M/B LA-5981P Schematic				Sheet 35 of 63			

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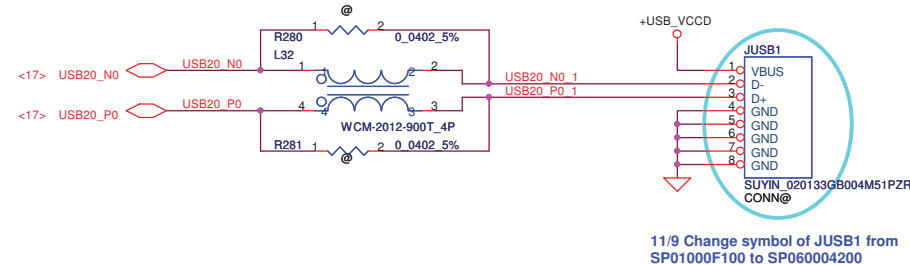
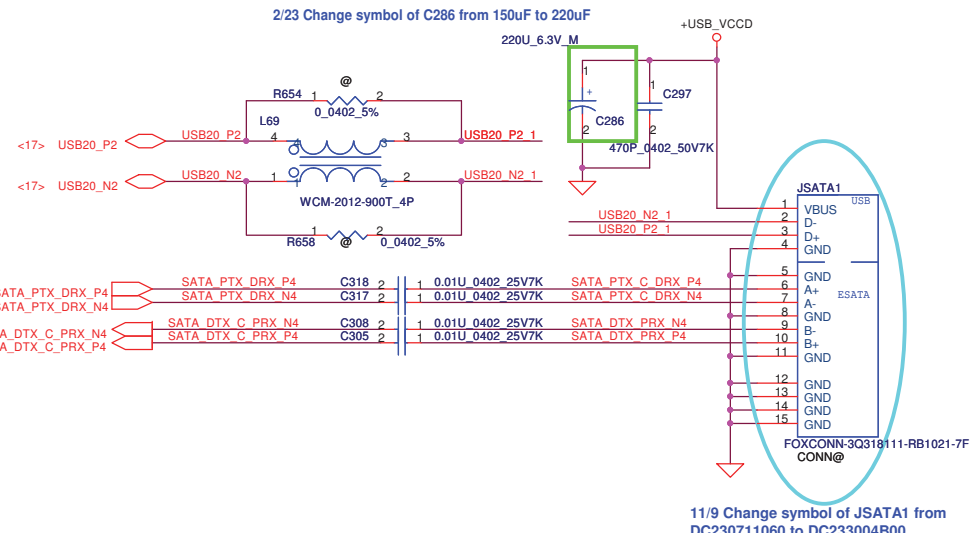
eSATA



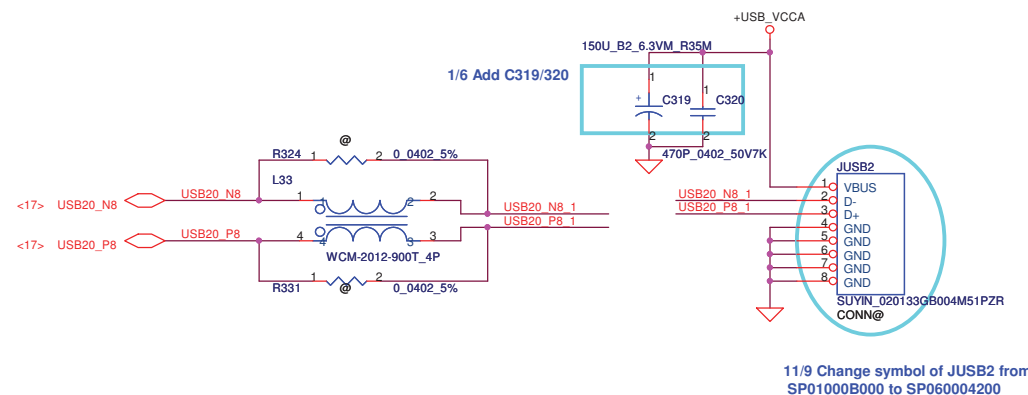
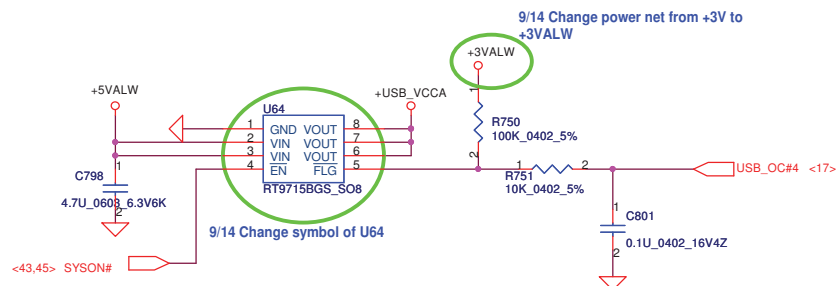
10/28 Add symbol of D16 of SC300000P00



10/28 Change symbol of D13 from SC300000000 to SC300000P00

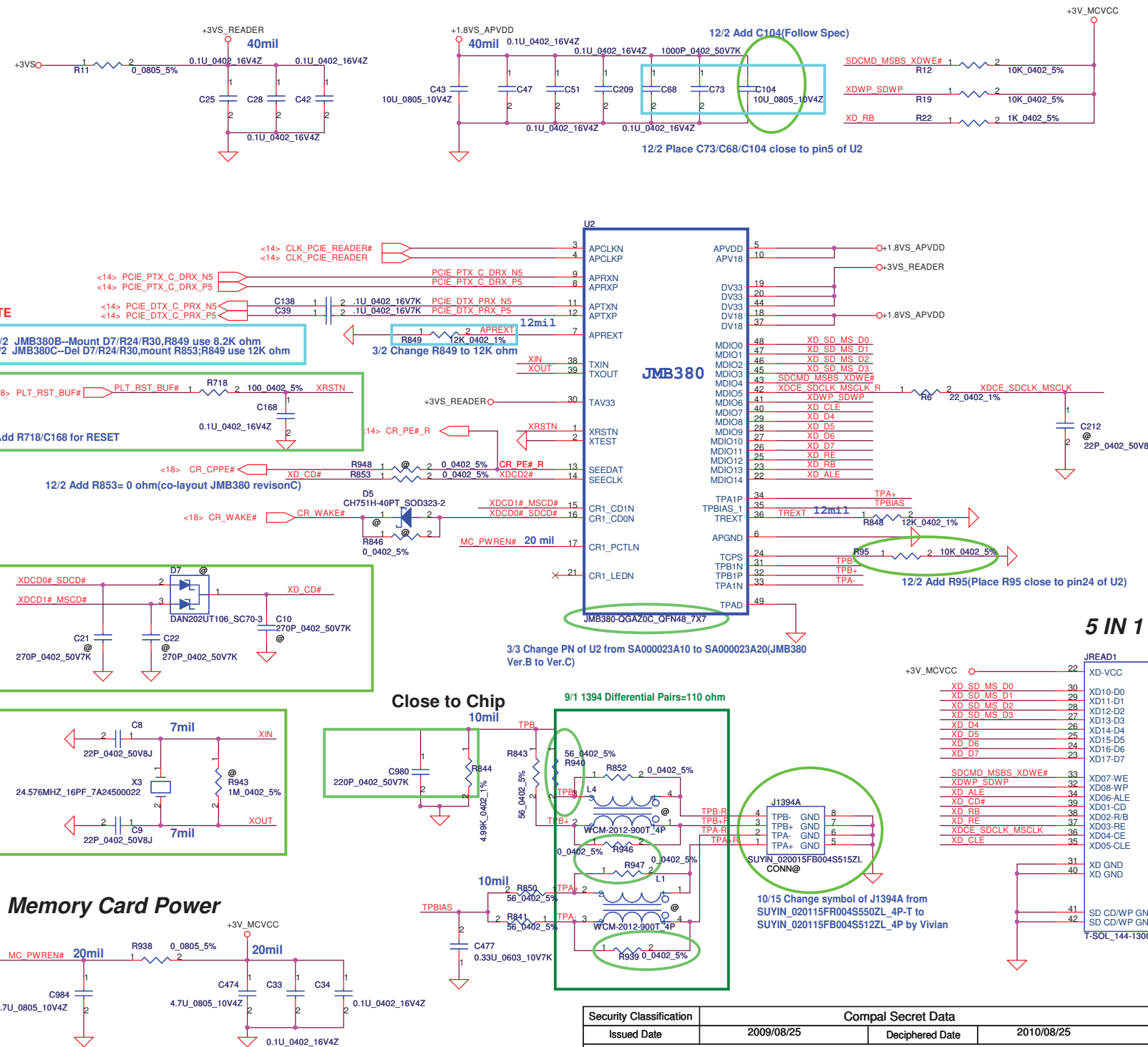


HS USB Port



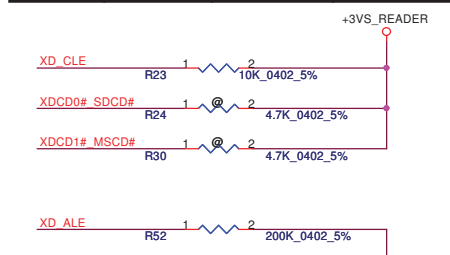
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				Size	Document Number	Rev	
				Custom	NCQF0 M/B LA-5981P Schematic	1.0	
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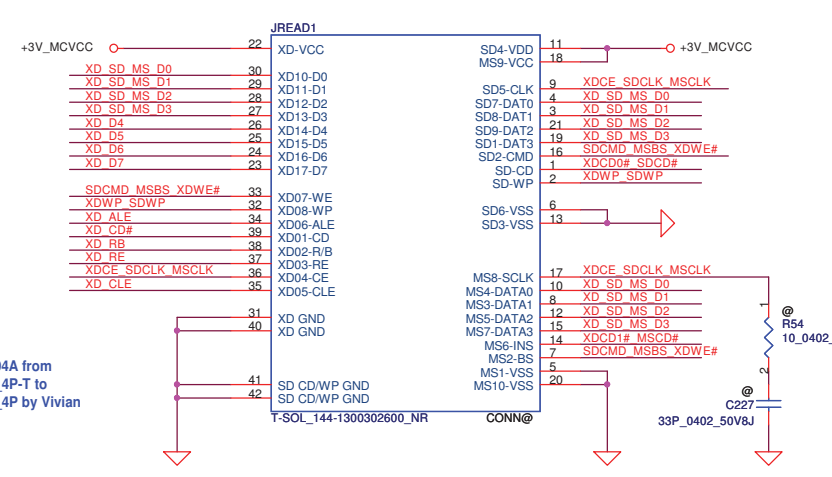


SD,MMC,MS, xD multi-function pin define

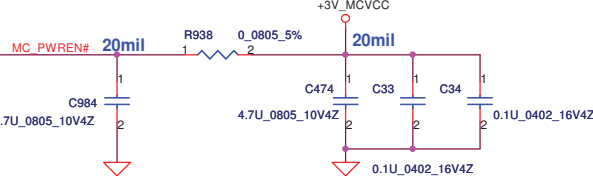
MDIO PIN Name	SD/MMC PIN Name	MS Card PIN Name	xD Card PIN Name
MDIO00	SD7-DAT0	MS4-DATA0	XD10-D0
MDIO01	SD8-DAT1	MS3-DATA1	XD11-D1
MDIO02	SD9-DAT2	MS5-DATA2	XD12-D2
MDIO03	SD1-DAT3	MS7-DATA3	XD13-D3
MDIO04	SD2-CMD	MS2-BS	XD07-WE
MDIO05	SD5-CLK	MS8-SCLK	XD04-CE
MDIO06	SD-WP		XD08-WP
MDIO07			XD05-CLE
MDIO08			XD14-D4
MDIO09			XD15-D5
MDIO10			XD16-D6
MDIO11			XD17-D7
MDIO12			XD03-RE
MDIO13			XD02-R/B
MDIO14			XD06-ALE
CR1_LEDN			
CR1_PCTLN			
CR1_CD0N	SD-CD		XD01-CD
CR1_CD1N		MS6-INS	XD01-CD



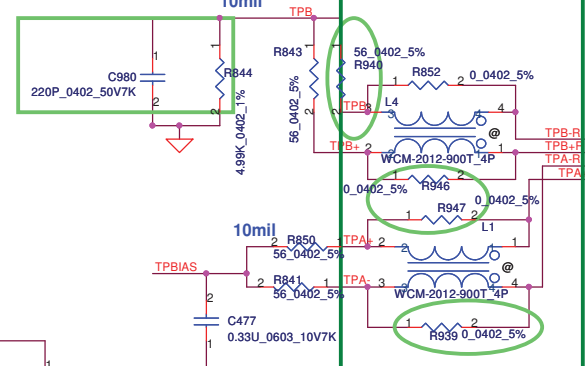
5 IN 1 CardRead



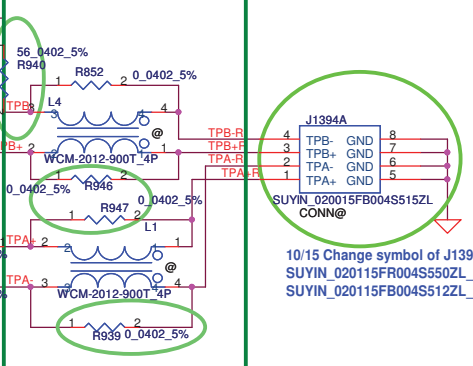
Memory Card Power



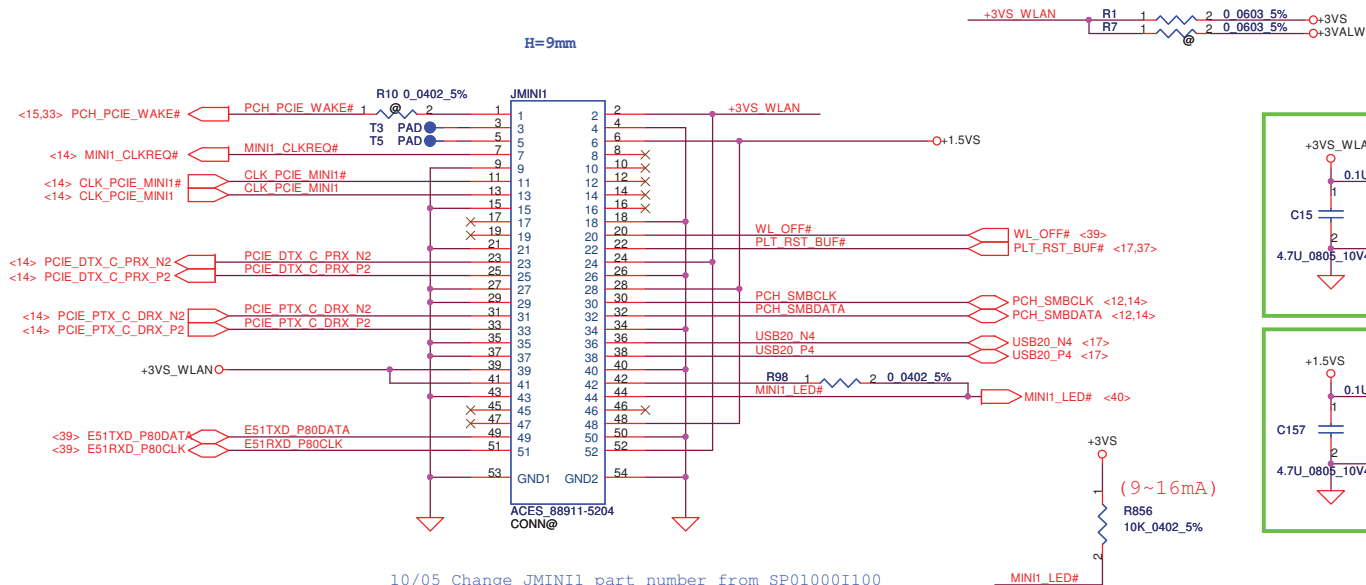
Close to Chip



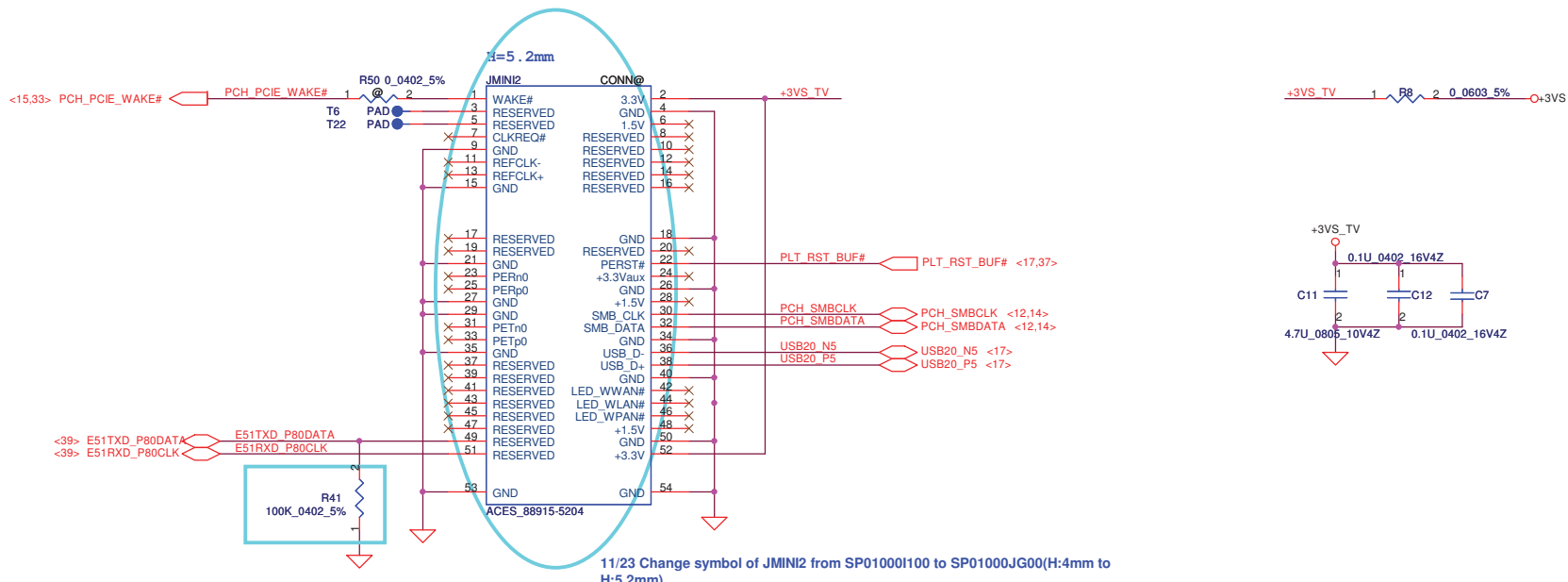
9/11 1394 Differential Pairs=110 ohm



WLAN



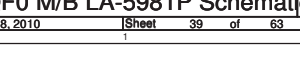
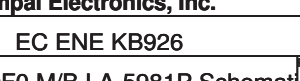
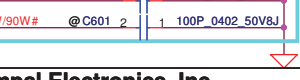
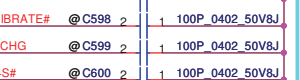
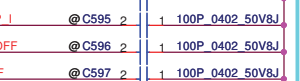
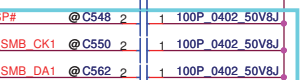
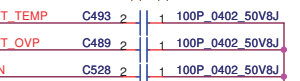
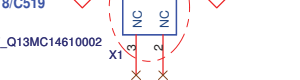
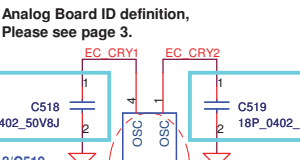
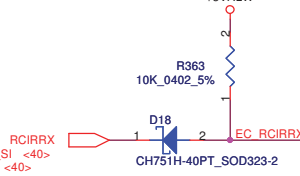
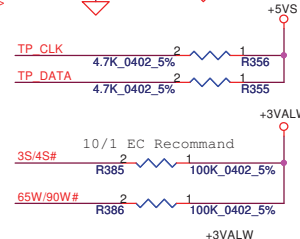
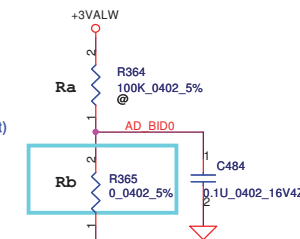
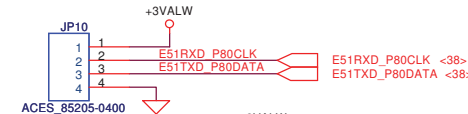
MINI



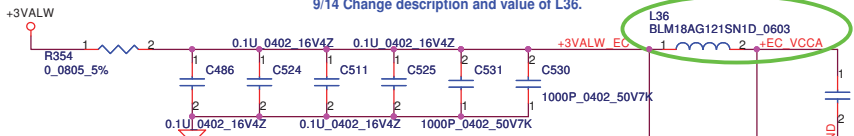
11/9 Change symbol of R41 from SD028100280 to SD028100380(10k ohm to 100k ohm)

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Document Number				NCQF0 M/B LA-5981P Schematic	
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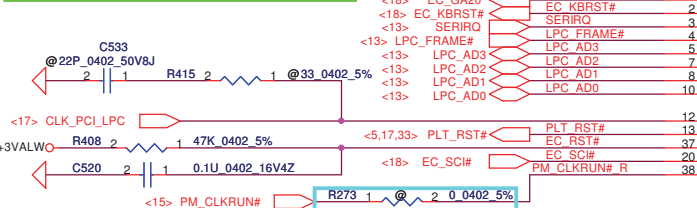
For EC Tools



9/14 Change description and value of L36.



9/14 Add By Vivian(EMI suggest)
0.1U 0402 16V4Z 2 1 @ EC_KBRST#
C535



11/11 Add R273=@ 0 ohm(Follow NAU00)

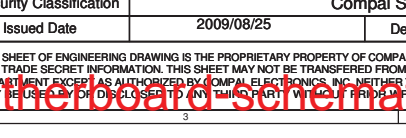
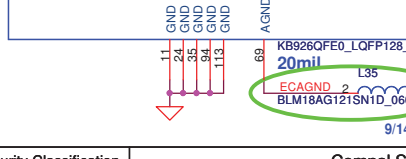
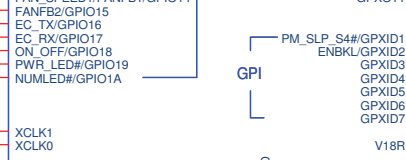
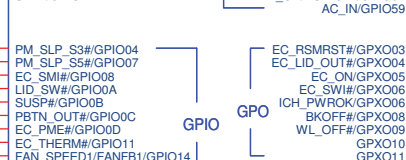
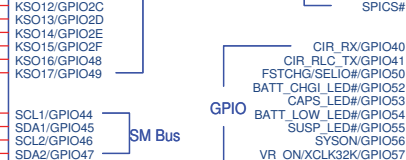
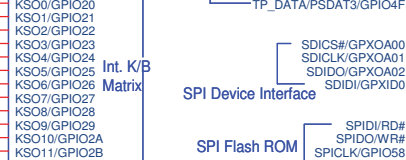
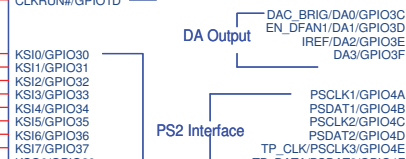
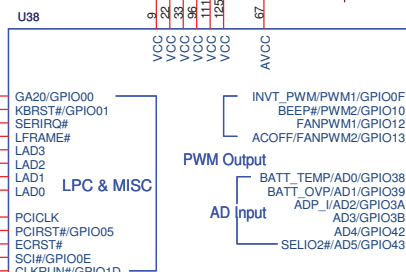
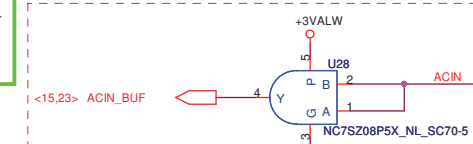
2/25 Add R430/R442/R446

2/25 Change Bom structure of R421/R422/R431 from mount to @

11/9 Add R459

4/15 Change PN of SW2/SW3 from SN100001C00 to SN100003R00

4/1 Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P



12/11 Change PN of U38 from SA00001J580 to SA00001J5A0(Rev:D3 to E0)

12/ 11 Change R365 from 100K to 0 ohm(Follow EC request)

9/1 Change net to ENCODER_DIR

1/14 Change value of C518/C519 from 15pF to 18pF

12/8 Add C548/C550/C562/C595-C601=@ 100pF(Avoid switching noise)

9/14 Change description and value of L35.

9/14 Change description and value of L35.

9/14 Change description and value of L35.

9/14 Change description and value of L35.

9/14 Change description and value of L35.

9/14 Change description and value of L35.

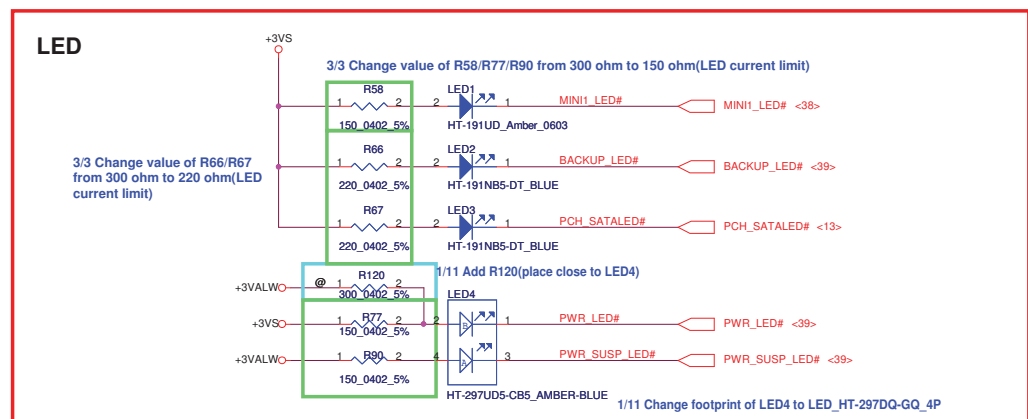
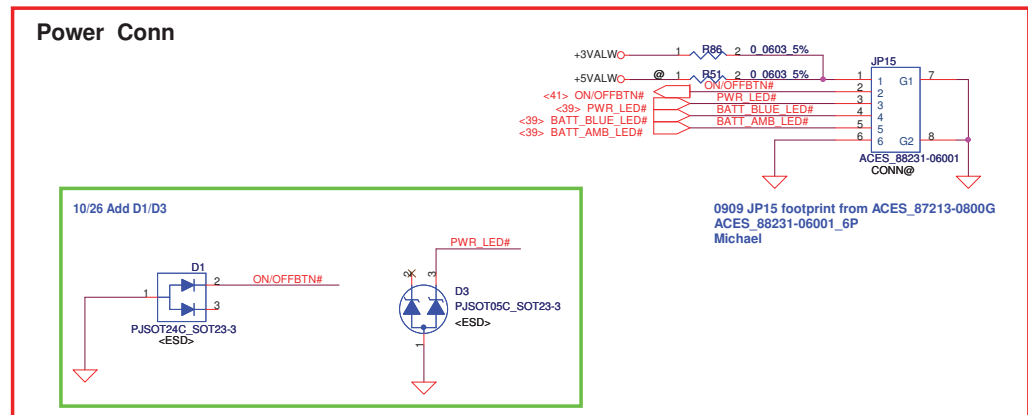
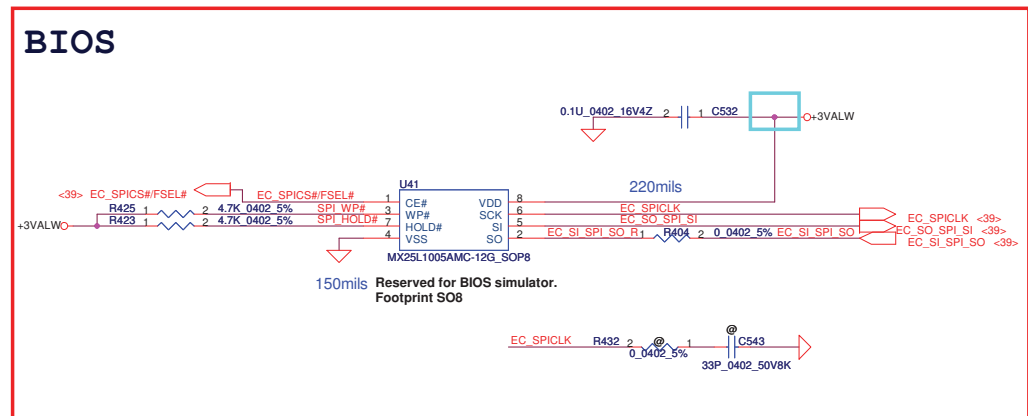
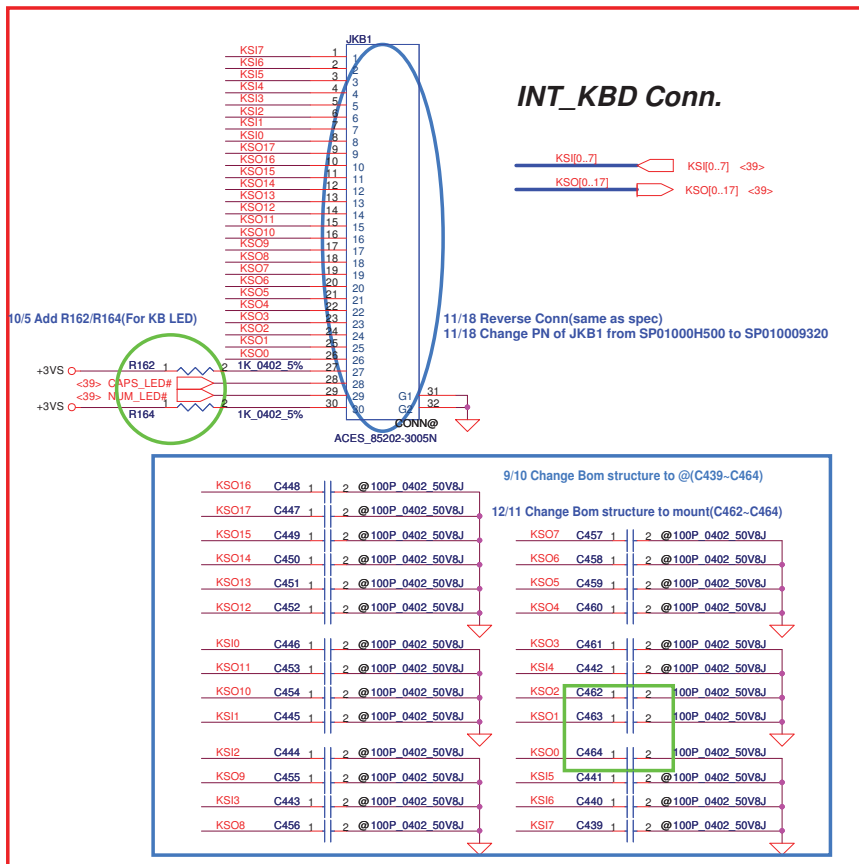
9/14 Change description and value of L35.

9/14 Change description and value of L35.

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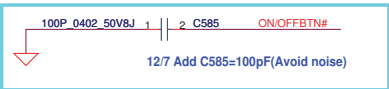
Compal Electronics, Inc.			
EC ENE KB926			
Size	Document Number	Rev	
B	NCQF0 M/B LA-5981P Schematic	1.0	
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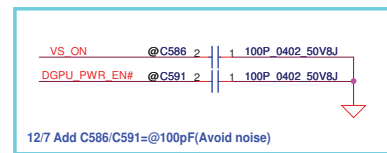
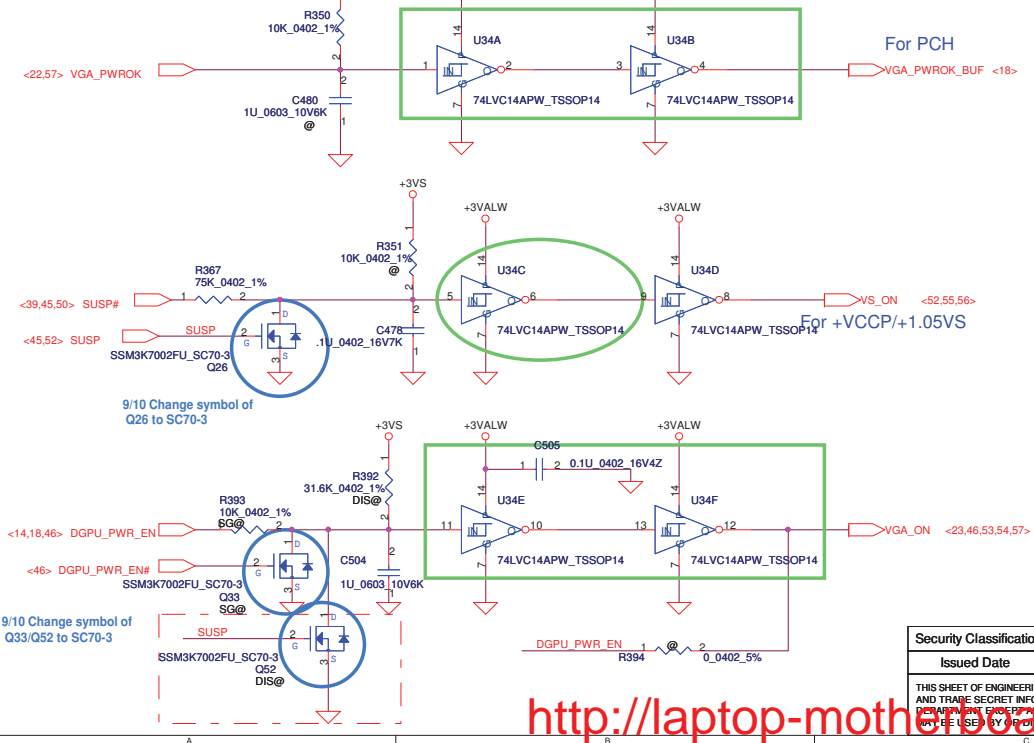


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				Rev	NCQF0 M/B LA-5981P Schematic
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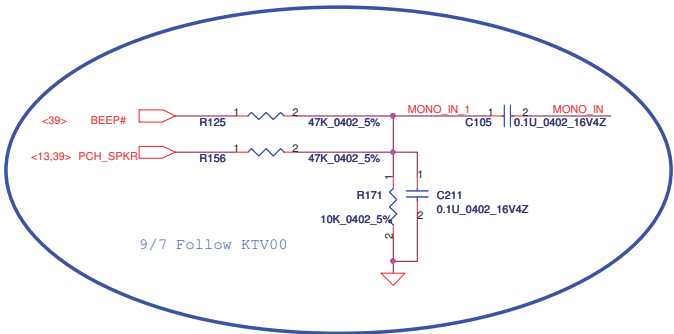
Power Button



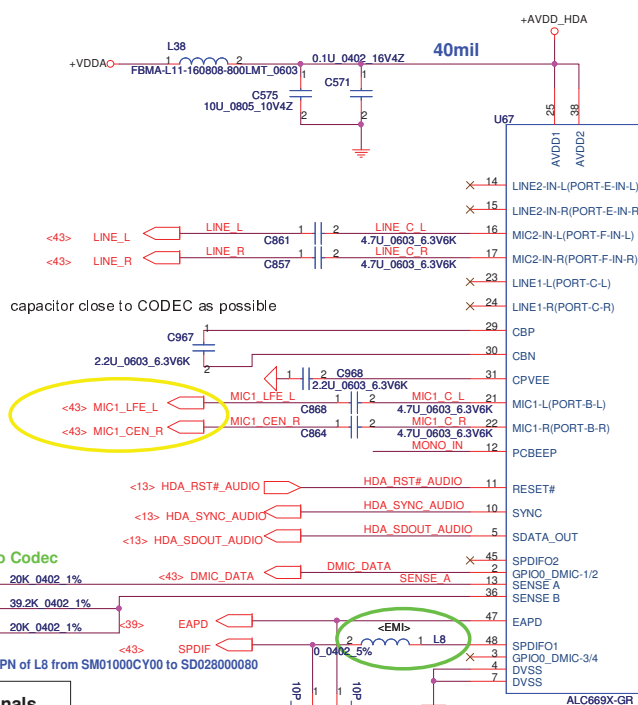
Power ON Circuit



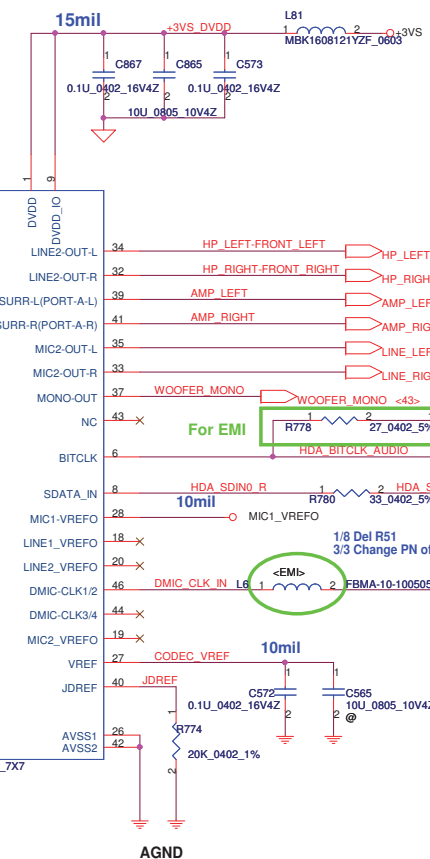
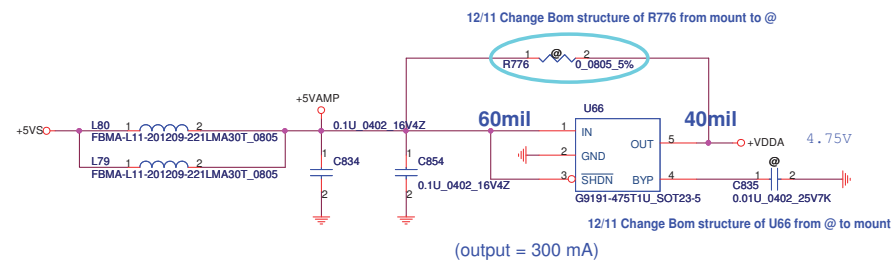
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Issued Date		2009/08/25		Deciphered Date		2010/08/25	
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				Power OK/PBN/TP Lock/LED			
				Size	Document Number		Rev
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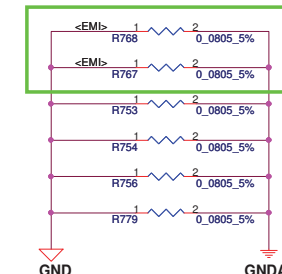
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	20K	PORT-A (PIN 39, 41)
		PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)



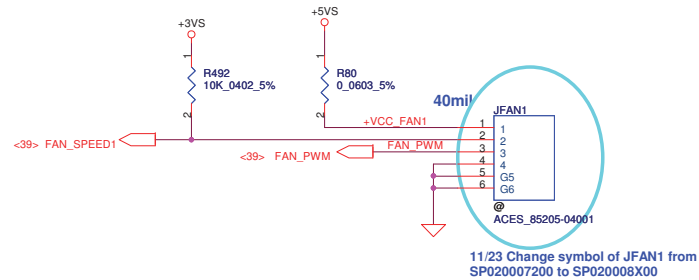
9/14 Add By Vivian(EMI suggest)



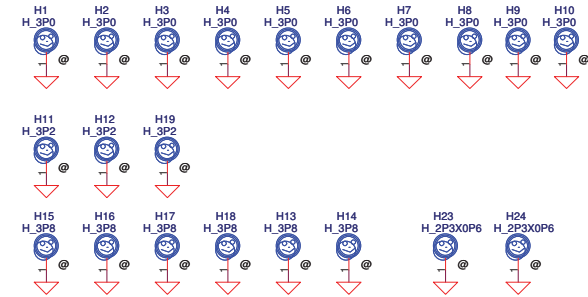
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Size	B	Document Number	NCQF0 M/B LA-5981P Schematic	Rev 1.0	
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FAN1 Conn

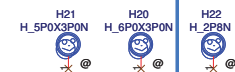


Screw



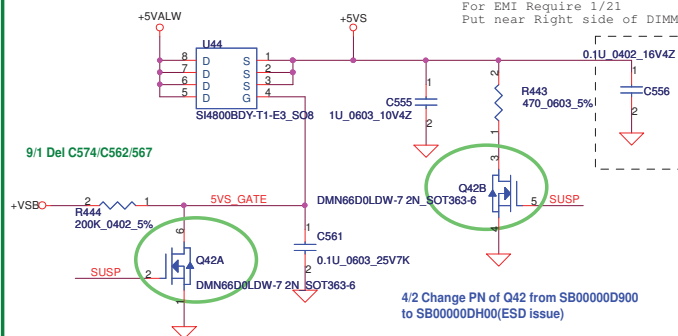
NON-PDH

2/25 Change footprint of H22

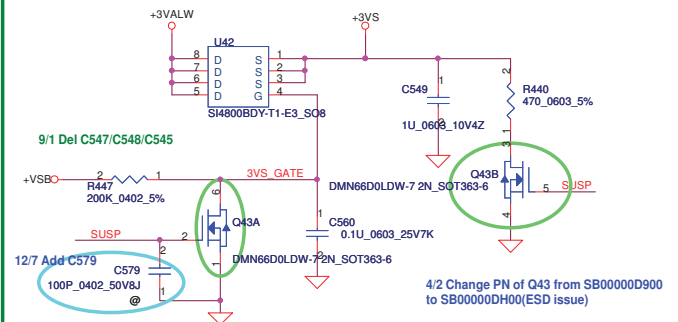


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+5VALW TO +5VS

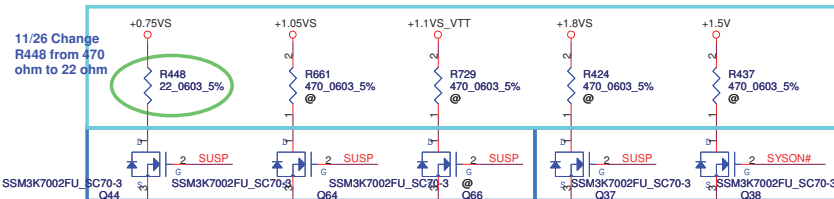
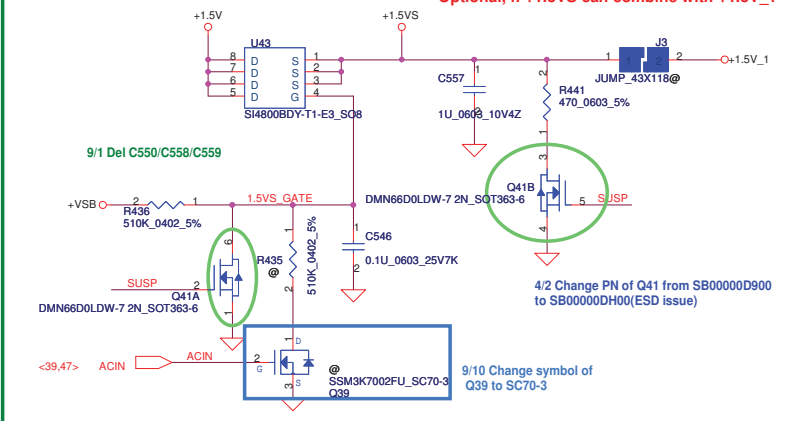


+3VALW TO +3VS

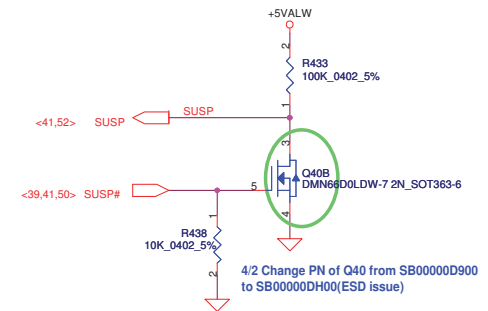
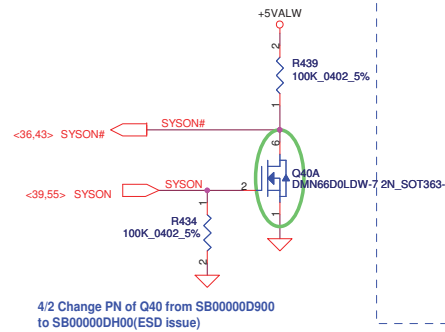


+1.5V to +1.5VS

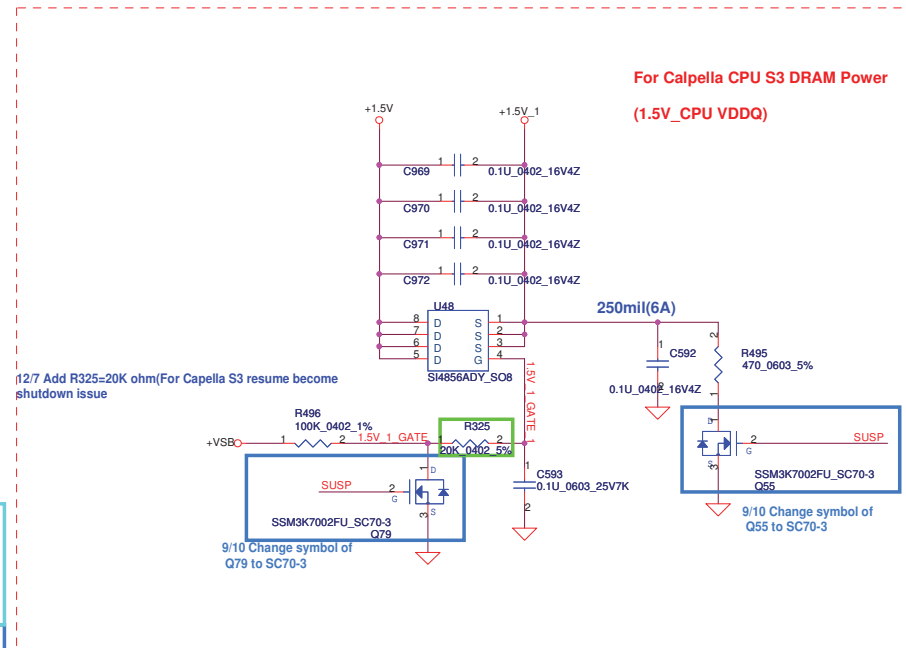
Optional, if +1.5VS can combine with +1.5V_1



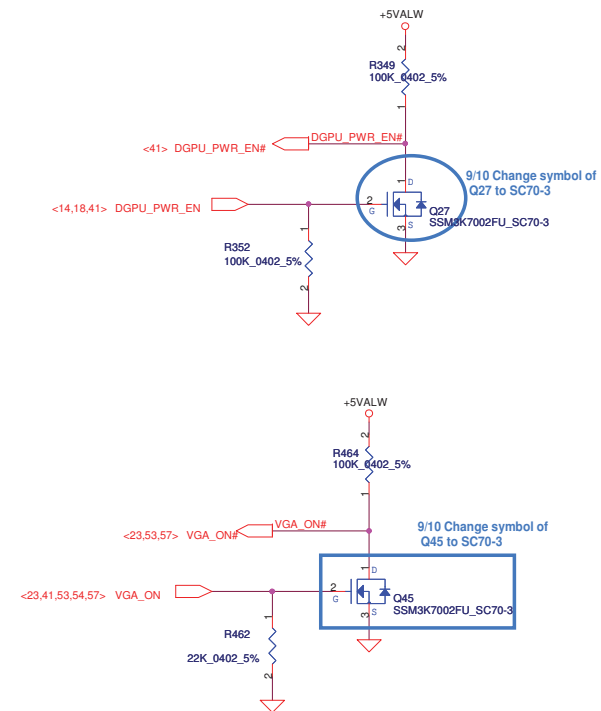
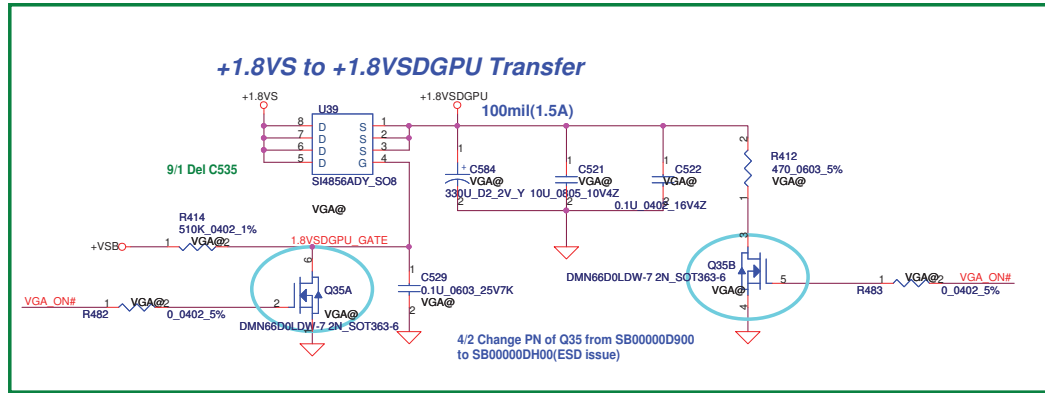
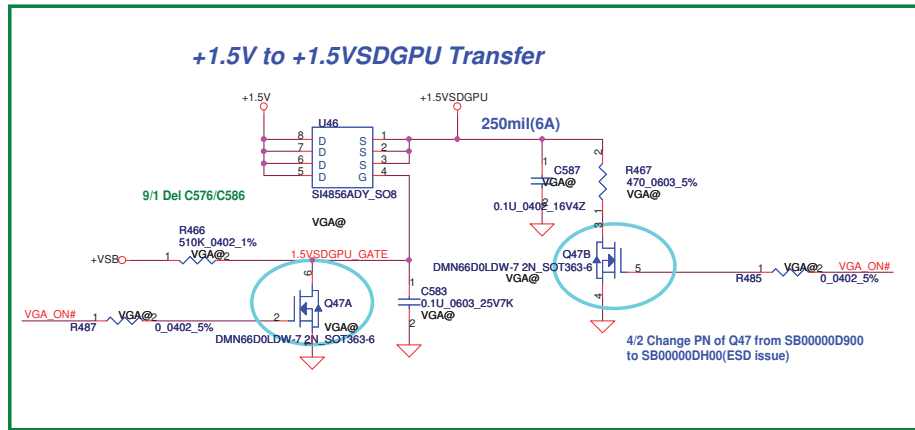
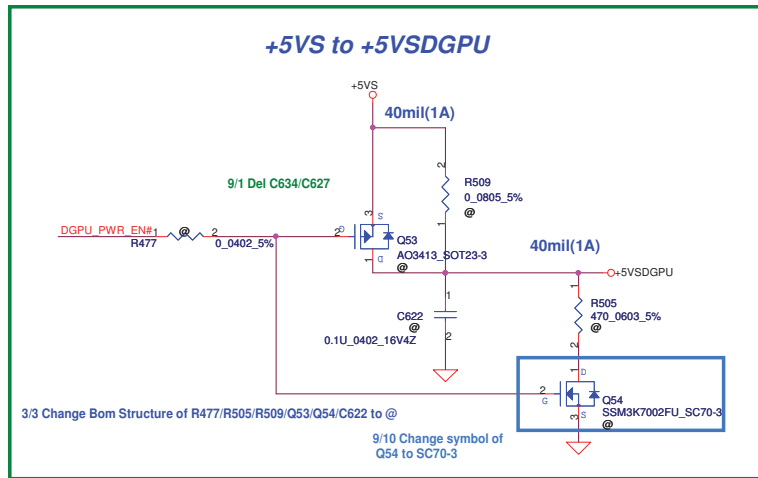
10/9 Delete R428, R431 and Q36
(Remove SBPWR_EN# Function)



For Calpella CPU S3 DRAM Power
(1.5V_CPU VDDQ)



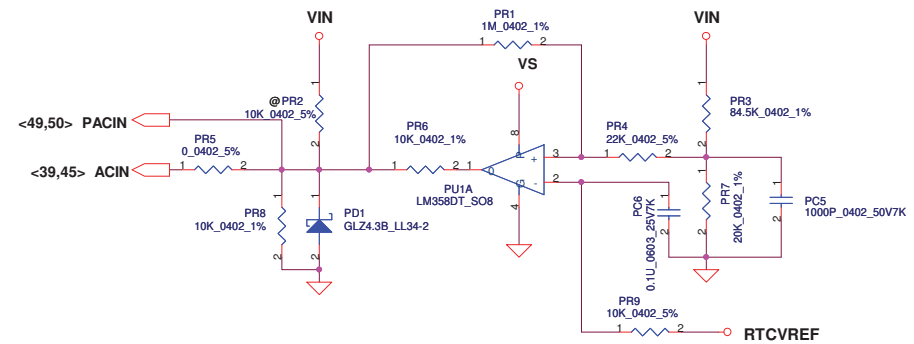
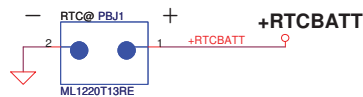
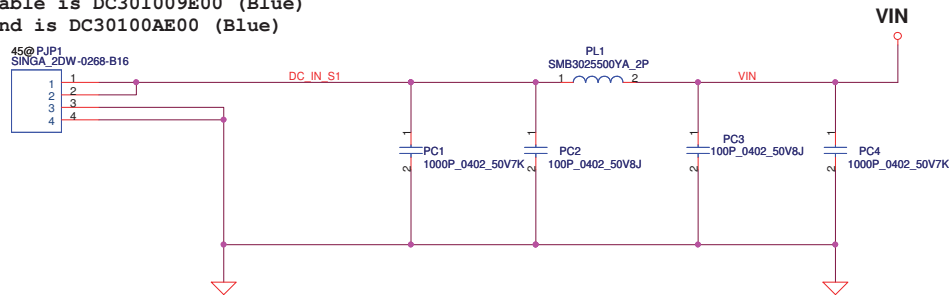
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								2010/08/25			
Title				DC Interface				NCQF0 M/B LA-5981P Schematic			
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				B	NCQF0 M/B LA-5981P Schematic
				Date:	Rev
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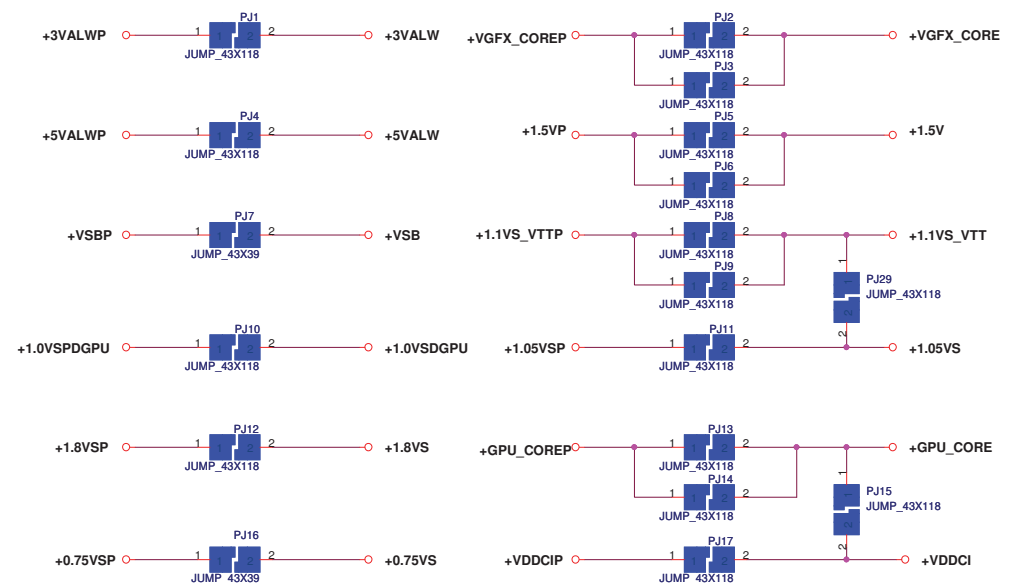
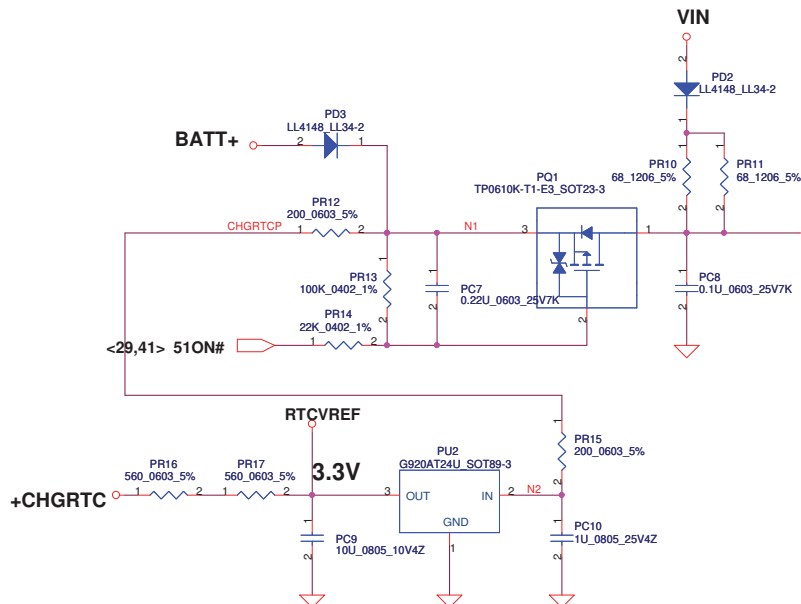
<http://laptop-motherboard-schematic.blogspot.com/>

On board conn is DC301001Y00
Cable is DC301009E00 (Blue)
2nd is DC30100AE00 (Blue)



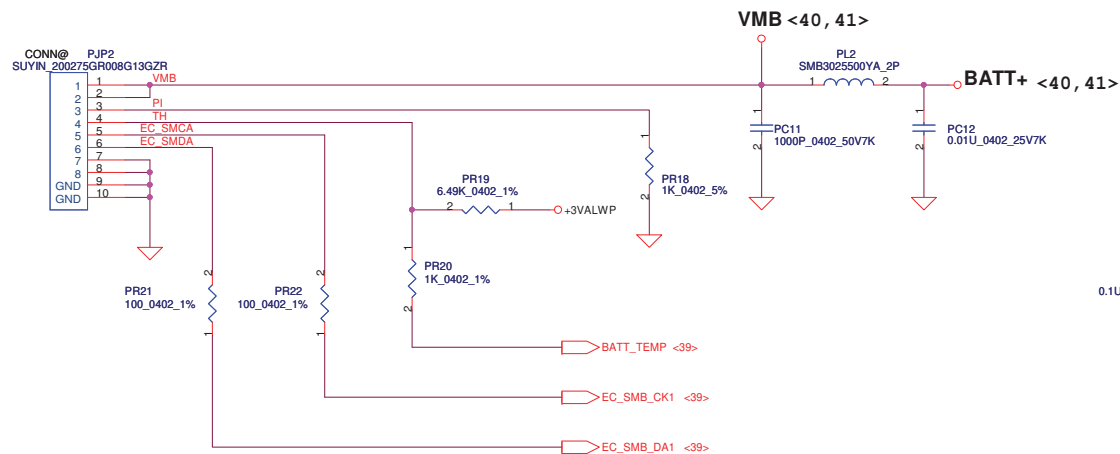
Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



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Size	Document Number	Customer	NCQF0 M/B LA-5981P Schematic	Rev	0.1
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Reference only!! Not SPEC

PH1 under CPU botten side :

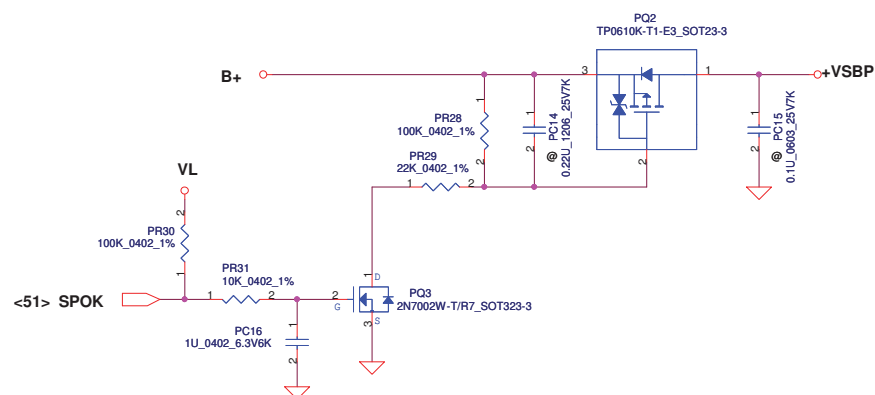
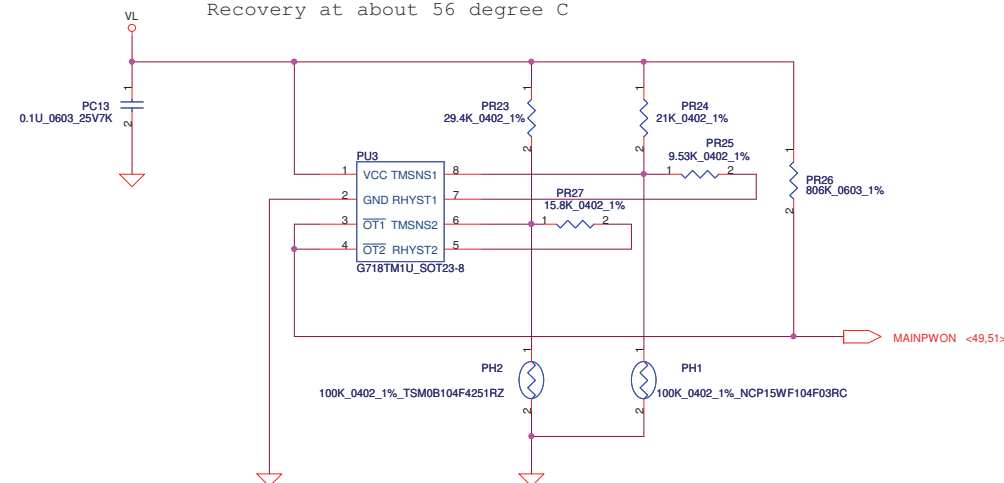
CPU thermal protection at about 92 degree C

Recovery at about 56 degree C

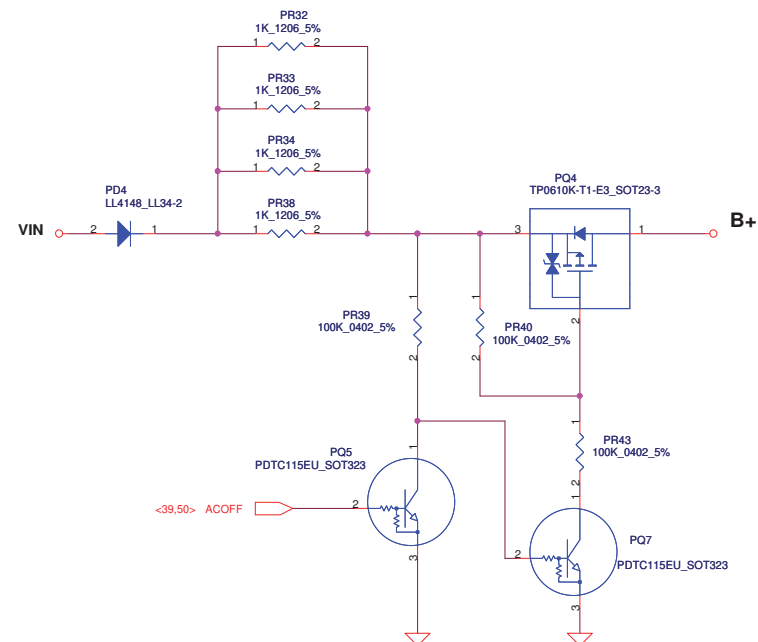
PH2 under FAN down side :

CPU thermal protection at about 82 degree C

Recovery at about 56 degree C



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				BATTERY CONN / OTP	
Size		Document Number		Rev	
Custom		NCQF0 M/B LA-5981P Schematic		0.	
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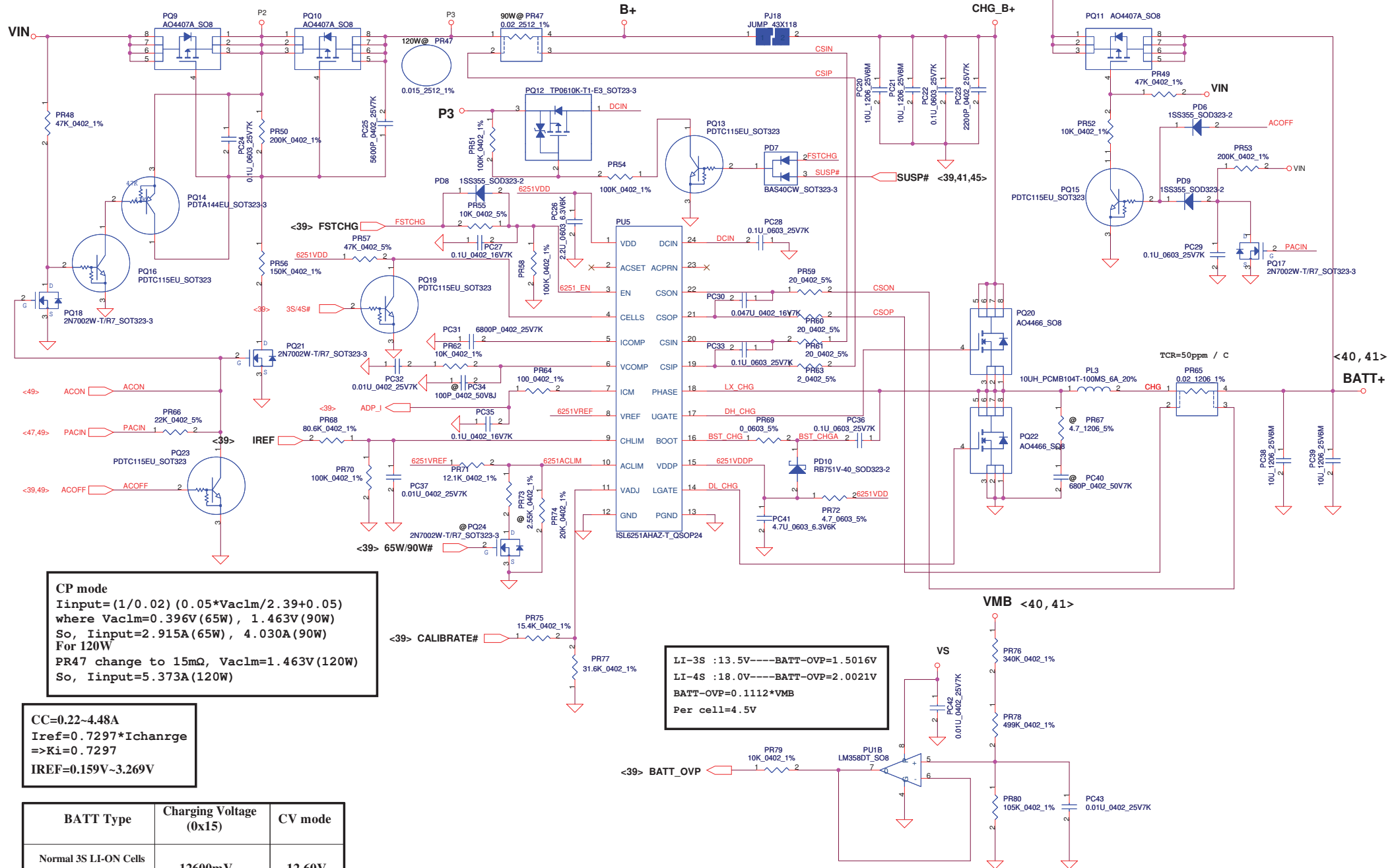


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Iada=0~4.74A (90W/19V=4.737A)
Iada=0~3.42A (65W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

90W: CP = 85%*Iada ; CP = 4.026A
65W: CP = 85%*Iada ; CP = 2.908A



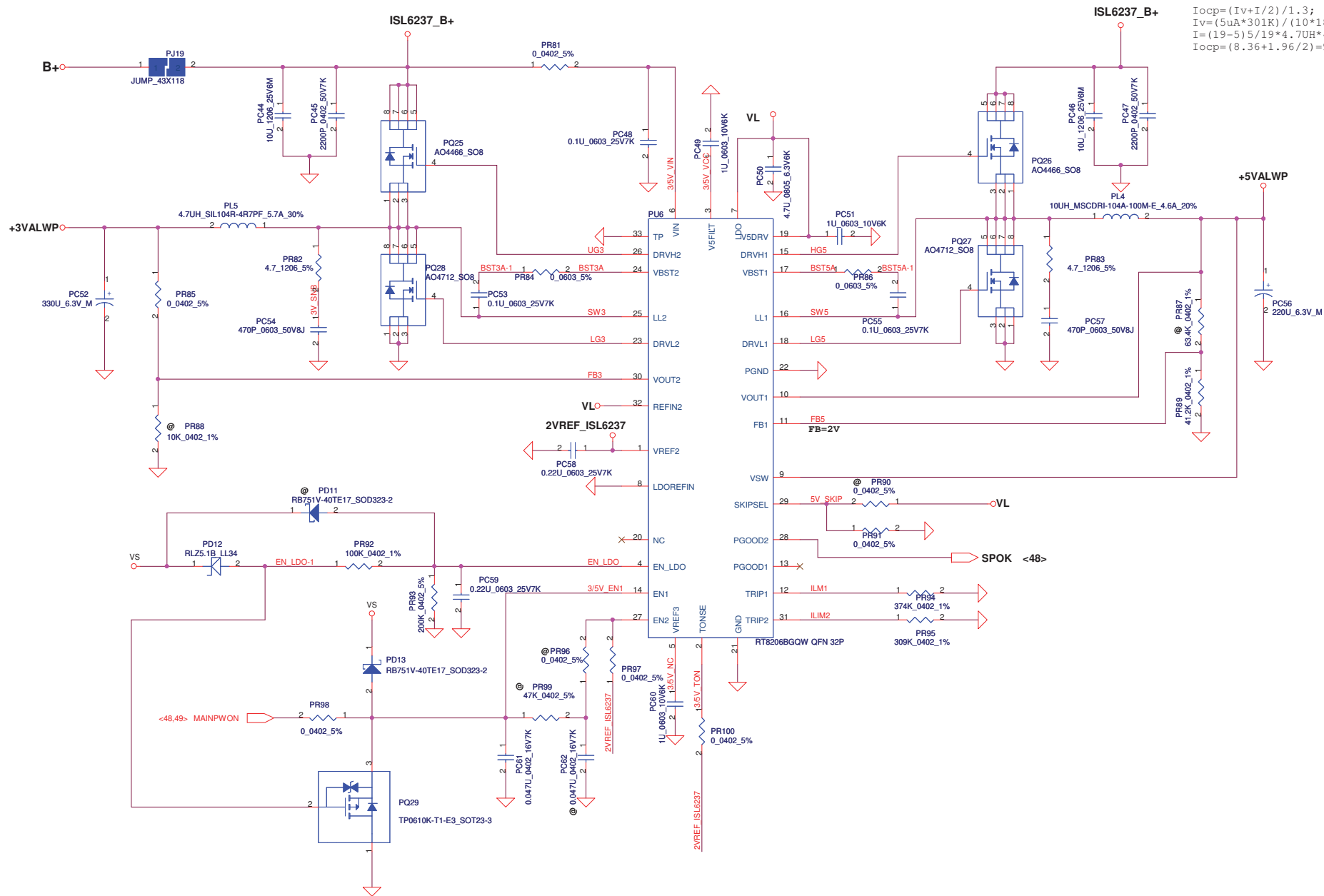
CP mode
 $I_{input} = (1/0.02) (0.05 * V_{ac1m} / 2.39 + 0.05)$
 where $V_{ac1m} = 0.396V$ (65W), $1.463V$ (90W)
 So, $I_{input} = 2.915A$ (65W), $4.030A$ (90W)
 For 120W
 PR47 change to 15mΩ, $V_{ac1m} = 1.463V$ (120W)
 So, $I_{input} = 5.373A$ (120W)

CC=0.22~4.48A
 $I_{ref} = 0.7297 * I_{charge}$
 $\Rightarrow Ki = 0.7297$
 $I_{REF} = 0.159V \sim 3.269V$

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

LI-3S : 13.5V----BATT-OVP=1.5016V
 LI-4S : 18.0V----BATT-OVP=2.0021V
 BATT-OVP=0.1112*VMB
 Per cell=4.5V

<http://laptop-motherboard.com/2010/08/25/ncqf0-m-b-la-5981p-schematic/>



$$I_{ocp} = (I_V + I_2) / 1.3;$$

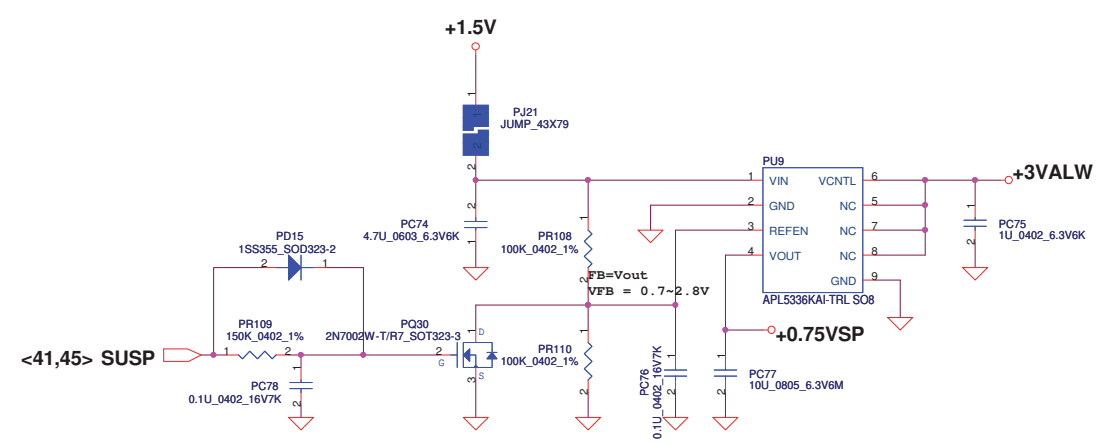
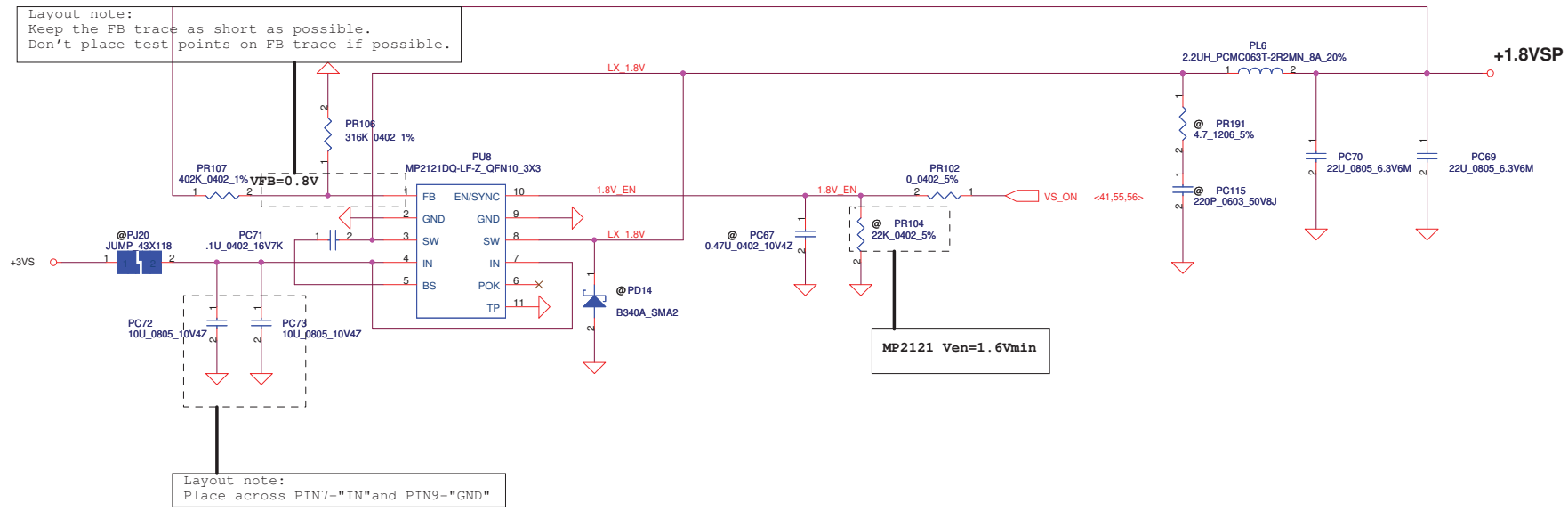
$$I_V = (5uA * 301K) / (10 * 18m) = 8.36A;$$

$$I = (19 - 5) / 19 * 4.7uH * 400K = 1.96A;$$

$$I_{ocp} = (8.36 + 1.96 / 2) = 9.34A$$

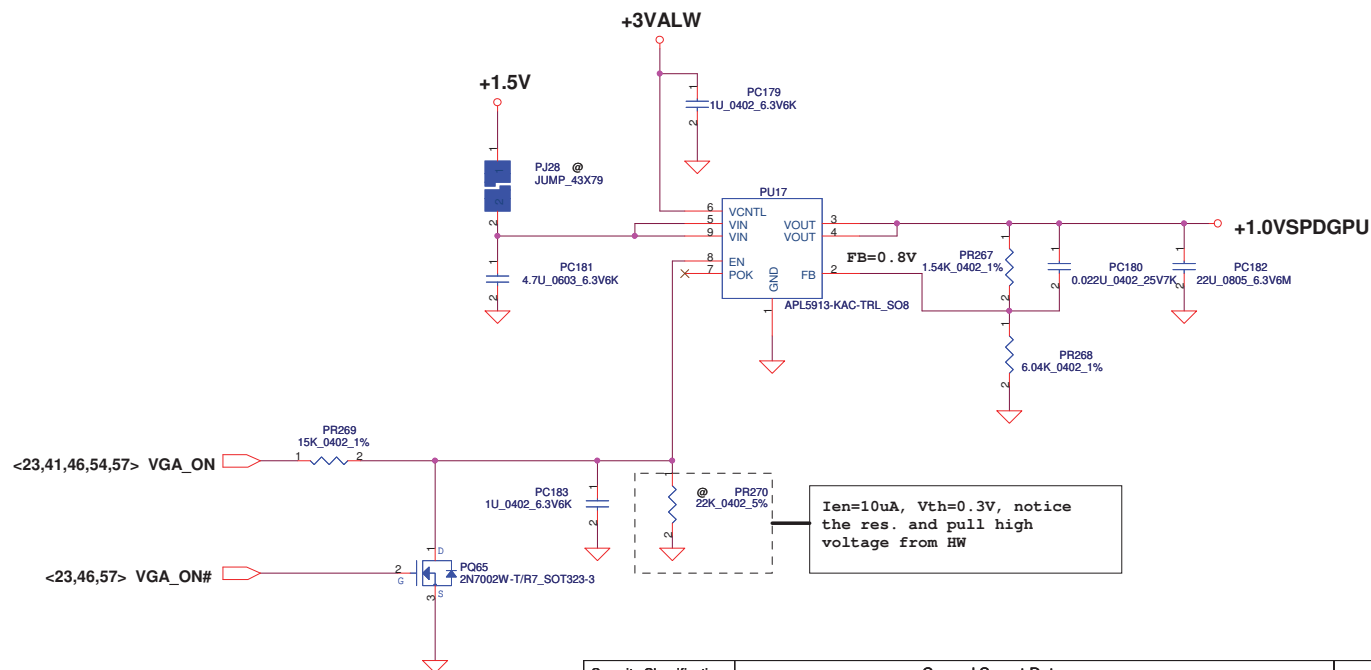
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Issued Date	2009/08/25	Deciphered Date	2010/08/25	Title	3VALW/5VALW
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http://laptop-motherboard.schematic.org/				NCQF0 M/B	LA-5981P Schematic
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Layout note:
Keep the FB trace as short as possible.
Don't place test points on FB trace if possible.



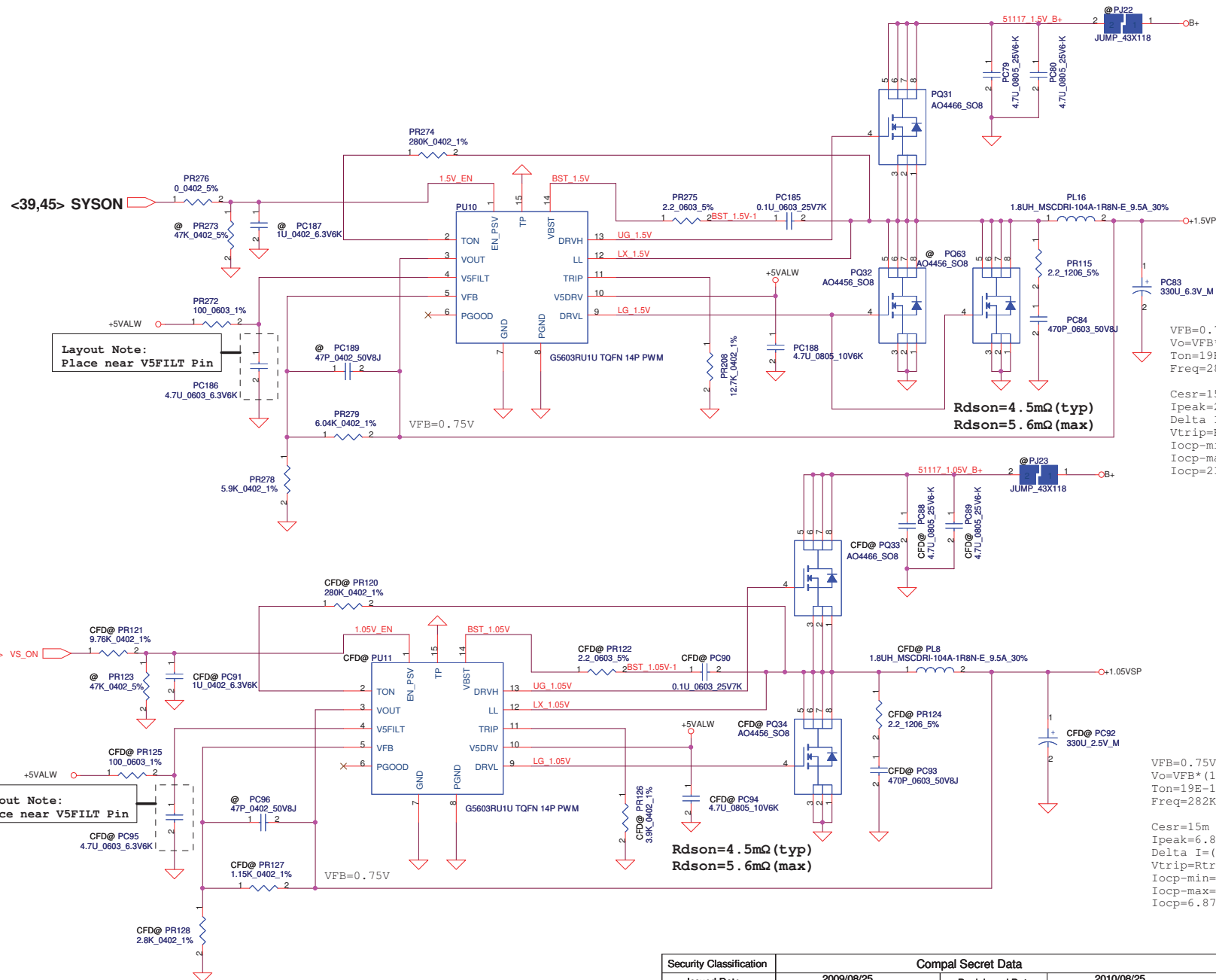
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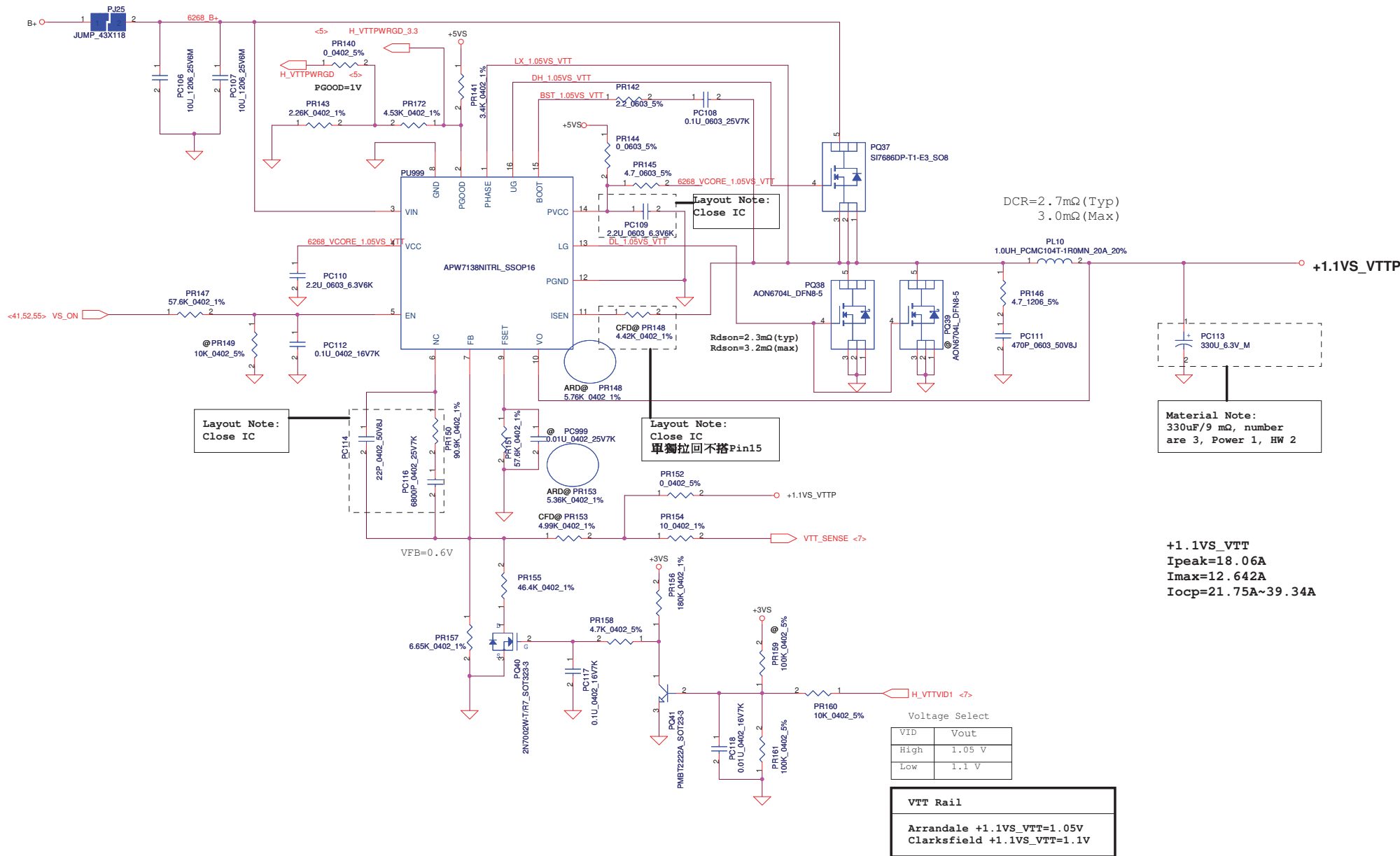
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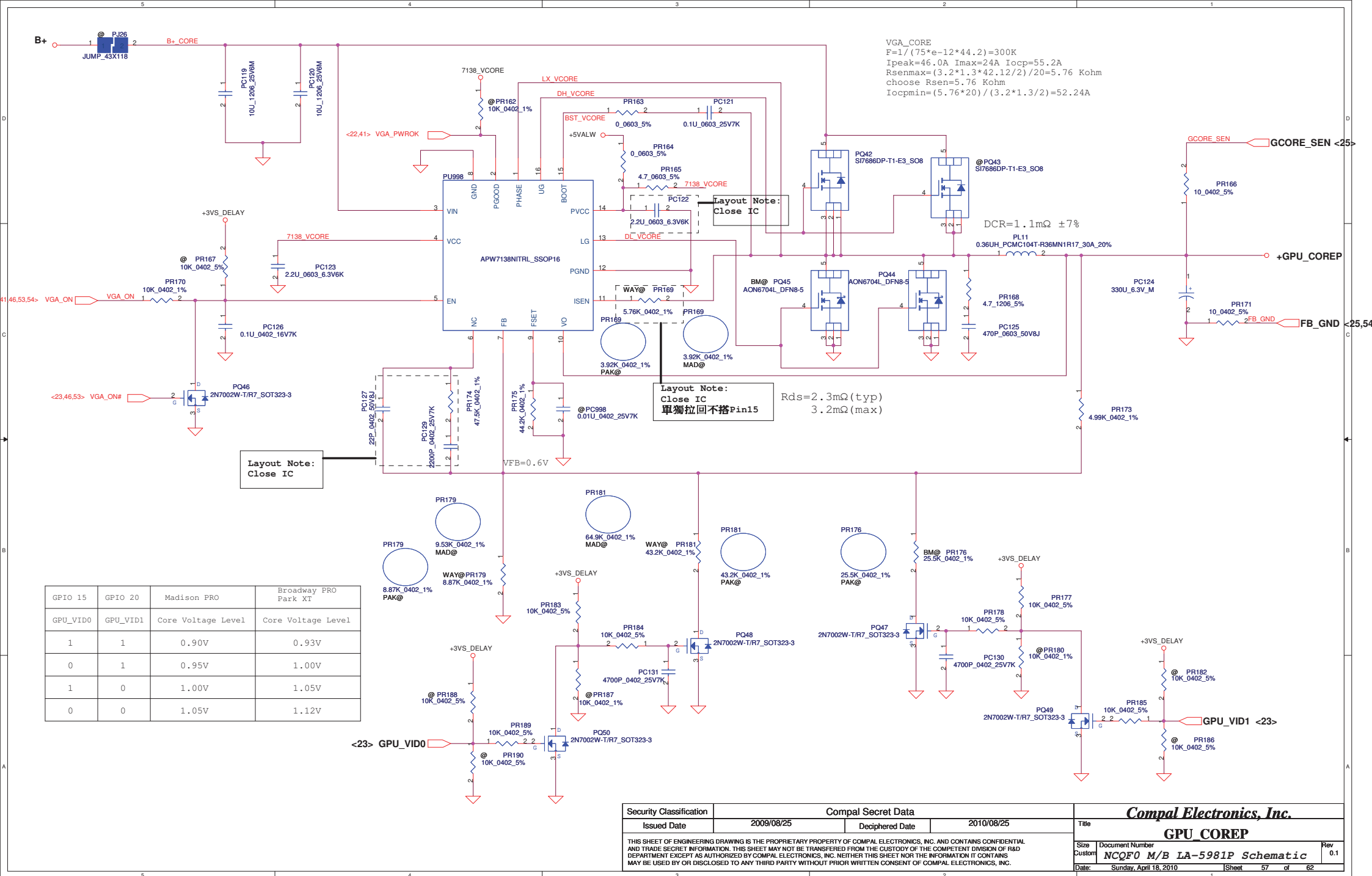


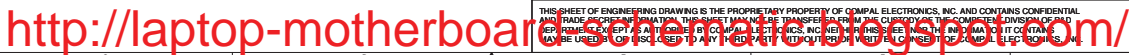
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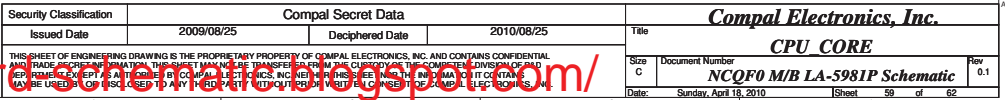
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	Design change	0.1	48	Change BQ24751 to ISL6251	2009 10/07	EVT
2	During shutdown, GFX has a pulse	Make GFX_EN pull down quickly	0.1	58	Add PD15 to connect GFX_EN and VS_ON	2009 11/02	EVT
3	Park XT SPEC change	More display performance	0.1	57	Change PR176 from 31.6kΩ to 43.2kΩ(SD034432280) Change PR179 from 9.53kΩ to 8.87kΩ(SD034887180) Change PR181 from 64.9kΩ to 25.5kΩ(SD034255280)	2009 11/05	EVT
4	ME height not enough	Prevent EL-cap. to knock the door	0.1	51	Change PC56 from 330uF 6L to 220uF 4.5L(SF0000002Y00)	2009 11/11	EVT
5	Cost review	Cost down	0.1	57	Change PC124 from 6mΩ to 10mΩ(SF0000002O00)	2009 11/11	EVT
6		Tune OCP	0.1	58	Change PR294 from 6.98kΩ to 7.15kΩ(SD034715180) Change PR299 from 10.7kΩ to 11kΩ(SD034110280)	2009 11/11	EVT
7		Tune OCP & Imon	0.1	59	Change PR239 from 499kΩ to 4.53kΩ(SD034453180) Change PC162 from 0.082uF to 0.1uF(SE076104KM8) Change PR258 from 1.91kΩ to 2.05kΩ(SD034205180) Change PR261 from 73.2kΩ to 74.5kΩ(SD034715280) Change PR263, PR264 from 120kΩ to 127kΩ(SD014127380) Change PR258 from 1.91kΩ to 2.05kΩ(SD034205180)	2009 11/11	EVT
8							
9	Not enough space	Not enough space	0.1	52	Change PL6 from 10x10 to 7x7(SH0000006I80)	2009 11/12	EVT
10	HW Jason request	Add new VGA voltage table	0.1	57	Add PR176, PR179, PR181 virtual parts	2009 11/19	EVT
11	Design review	1.5V change APW7138 to TPS51117	0.1	55		2009 11/19	EVT
12	Design review	Provide GFX output a reference	0.1	58	Add PR310, PR311	2009 12/03	EVT
13	S3 resume shutdown	Make sure 0.75V high later than 1.5V and low earlier than 1.5V	0.1	52	Add PD15	2009 12/08	EVT
14	Design review	1.5V tune output voltage	0.2	55	Change PR278 from 59kΩ to 124kΩ(SD034124380) Change PR279 from 24kΩ to 124kΩ(SD034124380) Change PR208 from 9.09kΩ to 16.9kΩ(SD034169280)	2009 12/15	DVT
15	Power OFF sequence	+1.0vsdgpu need power down within 20ms	0.2	53	Add PQ65	2010 01/05	DVT
16	HW request raise 1% voltage	1.5V tune output voltage	0.2	55	Change PR279 from 124kΩ to 127kΩ(SD034127380)	2010 01/07	DVT
17	OTP activity	Have a pull high	0.2	48	Enable PR23	2010 01/07	DVT
18	EMI solution	Add bypass cap from B+ to Gnd	0.2	59	Add PC184, PC190, PC204, PC205, PC206	2010 01/08	DVT
19	GFX character	Improve Imon, Loadline	0.2	58	Change PR294 from 7.15kΩ to 7.32kΩ(SD034732180) Change PR308 from 43.2kΩ to 53.6kΩ(SD034536380)	2010 01/08	DVT
20	CPU character	Improve Imon, Loadline, Transient	0.2	59	Change PR239 from 4.53kΩ to 4.42kΩ(SD0000004J80) Change PC176 from 390pF to 680pF(SE074681K80)	2010 01/08	DVT
21	Costdown	Change pack from 1206 to 0805	0.2		Change PC79, PC80, PC88, PC89, PC97, PC98 from 1206 to 0805(SE0000006R80)	2010 01/08	DVT
22	Tune sequence	GPU_core need ramp up before VDDCIP	0.2	54	Change PR131 from 10kΩ to 57.6kΩ(SD034576280)	2010 01/08	DVT
23	Run 3D Mark hang	Improve GPU character	0.2	57	Change PL11 from 0.56uH to 0.36uH(SH0000005680) Change PR169 from 2.43kΩ to 3.92kΩ(SD034392180) Change PR176 from 31.6kΩ to 25.5kΩ(SD034255280) Change PR184 from 68.1kΩ to 64.9kΩ(SD034649280) Change PR137 from 6.65kΩ to 7.87kΩ(SD034787180)	2010 01/13	DVT

Delete
2009
11/05

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MODIFICATION LIST

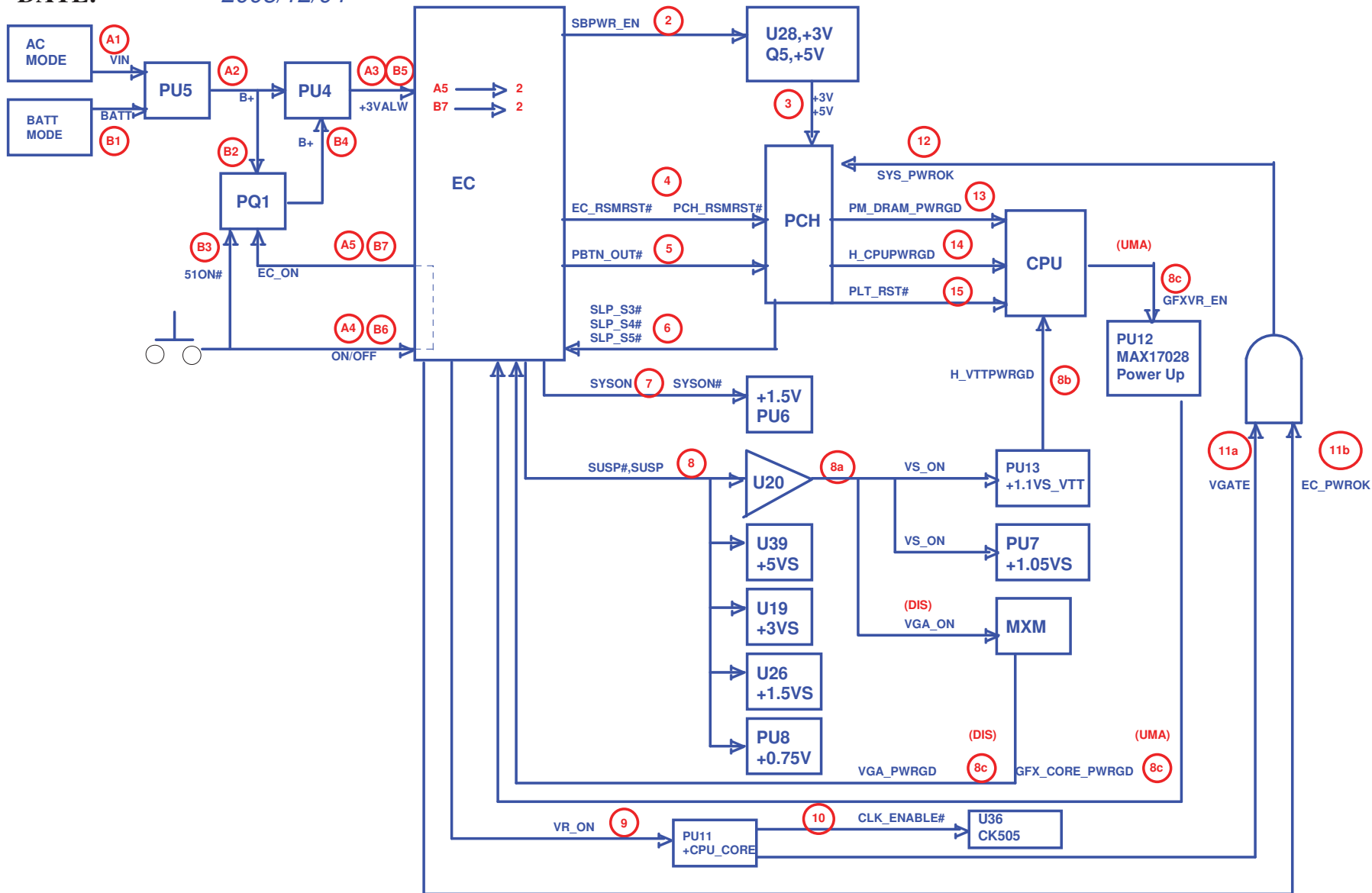
PURPOSE

01/05	P.40	PWR_LED# connect from +3VALW to +3VS; PWR_SUSP_LED# conector from +3VS to +3VALW
01/05	P.10	JDIMM1 and JDIMM2 location swap
01/05	P.47~60	upgrade PWR schematic
01/06	P.31	Change net name of Q85.pin2/5 from +3VS to +3VS_DELAY
01/06	P.35	Add one Lid Switch schematic for reserve
01/08	P.47~60	upgrade PWR schematic
01/08	P.42	Add two of 300 ohm bead for DMIC_CLK and SPDIF signal(L6/L8)
01/11	P.47~60	upgrade PWR schematic
01/11	P.40	Reserve R120=300 ohm pull-high to +3VALW
01/11	P.18	Change net name of Q23.pin2 from VGA_HDMI_DET to HDMI_HPD
01/12	P.25	Add C602=330uF to decrease ripple of +GPU_CORE
02/25	P.23	Change net connection(from R45.2 to Q7.1)
02/25	P.29	Add R37=SG@ 0 ohm connect between DPST_PWM_1 and INVTPWM
02/25	P.34	Add C936~C938=mount 0.1uF for slove EMI issue
02/25	P.39	Add R430/R442/R446=mount 10k ohm pull-high to +3VALW
02/25	P.39	Change Bom structure of R421/R422/R431 from mount to reserve
02/25	P.47~63	upgrade PWR schematic
03/01	P.5	Del XDP schematic(JP5/R89/R92/R93/R96/C168/R86/R657/R663)
03/01	P.14	Add R326/R345/R782/R796(for use JMB380 Ver.C)
03/01	P.14	Add Q49/Q50(for use JMB380 Ver.C)
03/01	P.47~63	upgrade PWR schematic
03/02	P.37	Add R718/C168 (for reset)
03/31	P.23	Add Update VRAM Table
03/31	P.43	Change value of R4 from 4.7K ohm to 5.62K ohm
03/31	P.43	Change value of C3 from 0.1uF to 0.033uF
03/31	P.36	Change Bom structure of R654/R658/R280/R281/R324/R331 from mount to @
03/31	P.36	Change Bom structure of L32/L33/L69 from @ to mount
03/31	P.36	Change symbol and PN of L32/L33/L39 from SM070001310 to SM070000K00
03/31	P.24	Change Bom structure of R83 from SG@ to MAD@
04/01	P.39	Change footprint of SW2/SW3 from SW_SKRELGE010_2P to SW_NTC317-AB1G-C220C_2P
04/02	P.23	Change PN of Q9 from SB00000D900 to SB00000DH00
04/02	P.29	Change PN of Q6/Q80/Q81 from SB00000D900 to SB00000DH00
04/02	P.30	Change PN of Q84 from SB00000D900 to SB00000DH00
04/02	P.31	Change PN of Q85 from SB00000D900 to SB00000DH00
04/02	P.31	Change PN of Q61 from SB570020110 to SB000008J10
04/02	P.43	Change PN of Q69 from SB00000D900 to SB00000DH00
04/02	P.45	Change PN of Q40/Q41/Q42/Q43 from SB00000D900 to SB00000DH00
04/02	P.46	Change PN of Q35/Q47 from SB00000D900 to SB00000DH00
04/15	P.39	Change PN of SW2/SW3 from SN100001C00 to SN100003R00
04/15	P.41	Change Bom structure of SW1 from mount to @
04/18	P.29	Add LVDS schematic(U13/U31/C204/C187=@)
04/18	P.40	Add R51=@ 0 ohm
04/18	P.47~63	upgrade PWR schematic

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MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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Version change list (P.I.R. List)

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	EMI request	Cut-in snubber and couple cap on B+	0.2		Enable 3V/5V/1.5V/1.05V/VTT/GPU snubber	2010 01/13	DVT
25	Buyer request	Costdown	0.2		Change PU10,PU11,PU12 from TPS51117 to G5603(SA00003HM00)	2010 01/14	DVT
26	HW/Ivan request	Raise voltage 2%(Arrendale only)	0.3	56	Change PR153 from 4.99KΩ to 5.36KΩ(SD034536180)	2010 02/11	PVT
27	The same setting for 2nd source	Fix 5V for all IC	0.3	51	Disable PR87	2010 02/23	PVT
28	GPU output cap add 330uF for hang issue	Tune VDDCIP sequence and Power common design	0.3	54	Change PR131 from 57.6KΩ to 301KΩ(SD034301380) Net +5VALW instead of +5VSDGPU	2010 02/23	PVT
29	EMI request	Cut-in snubber and boost res.	0.3		Change PR122,PR142,PR236,PR249,PR275 from 0Ω to 2.2Ω(SD013220B80) Add PR238,PR251 to 4.7Ω Add PC161,PC173 to 470pF	2010 02/25	PVT
30	65/90# only low signal	Fix adapter mode	0.4	50	Disable PR73, PQ24	2010 03/23	Pre-MP
8	Protect logic deformation	Add PH2 function	0.4	48	Change PR23 from 0Ω to 29.4Ω(SD034294280) Add PR27, PH2	2010 03/23	Pre-MP
9	Improve anti-noise	Reduce voltage divider	0.4	54	Change PR138 from 43K to 2.05K(SD034205180) Change PR139 from 124K to 5.9K(SD034590180) Change PR283 from 60.4K to 2.87K(SD034287180)	2010 03/26	Pre-MP
10	Improve anti-noise	Reduce voltage divider	0.4	55	Change PR278 from 124K to 5.9K(SD034590180) Change PR279 from 127K to 6.04K(SD034604180) Change PR127 from 24K to 1.15K(SD034115180) Change PR128 from 59K to 2.48K(SD034288180)	2010 03/26	Pre-MP
11							
12	Cut-in 120W adapter	Tune a CP setting for 120W adapter	0.4	50	Change PR47 from 0.02 to 0.015(SD000001E00)	2010 03/26	Pre-MP
13	Modify VGA voltage table	Rise Broadway voltage to the same to Park	0.4	57	Change PR179 from 9.53 to 8.87 Change PR181 from 64.9 to 43.2	2010 04/16	Pre-MP
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